MITSUBISHI

PROGRAMMABLE CONTROLLER

MELSEC-A

User's Manual

Computer link module type A1SJ71C24-R2
Computer link/Printer function module type A1SJ71C24-PRF

MITSUBISHI ELECTRIC

REVISIONS

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INTRODUCTION

Thank you for choosing the Mitsubishi MELSEC-A Series of General Purpose Programmable Controllers. Please read this manual carefully so that the equipment is used to its optimum. A copy of this manual should be forwarded to the end User.

CONTENTS

[COMMON]

[PRINTER FUNCTIONS]

[TROUBLESHOOTING]

Manual Contents and Model Names

(1) Manual Contents

This manual is divided into the following five general areas:

(a) Common (Sections 1 to 4):

Describes items common to computer link or printer functions such as the general description of operations, features, system configurations, general specifications, performance specifications, and setting and procedures before starting operations.

(b) Computer Link Functions (Sections 5 to 10):

Describes the method for communications using the computer link, the method for linking with a computer, and commands.

(c) Printer Functions (Section 11)*:

Describes the registration, reading, and output of messages when printer functions are used with an A1SJ71C24-PRF.

(d) Troubleshooting (Section 12):

Describes troubleshooting procedures if an error occurs when a CPU function, computer link function, or printer function is used.

(e) Appendices:

Describes compatibility with an A1SJ71C24-S6, the communications time between a CPU and computer link, and A-series special-function module buffer addresses.

* Printer functions are not explained at all in section of Computer Link Functions. Read the Printer Functions section when a printer function is used.

(2) Model Names

The following abbreviations are used in this manual:

- A1SJ71C24-R2:

  A1SJ71C24-R2 computer link module.

- A1SJ71C24-PRF:

  A1SJ71C24-PRF computer link and printer function modules.

- A1SJ71C24:

  A1SJ71C24-R2 computer link module and the A1SJ71C24-PRF computer link and printer function modules.

[COMMON]

The following sections explain the general description, features, system configurations, general specifications, performance specifications, and setting and procedures for operation of an A1SJ71C24-R2 and A1SJ71C24-PRF which are common to the computer link functions and printer functions.

1. GENERAL DESCRIPTION

This User's Manual describes the specifications, handling and transmission control protocols of the A1SJ71C24-R2 computer link module and the A1SJ71C24-PRF computer link/printer function module used together with a MELSEC-A Series A1SCPU.

The A1SJ71C24-R2, A1SJ71C24-PRF has one RS-232C port. It is the interface between a A1SCPU and an external device (such as a computer or printer) or to the CPU of another PC station.

Dedicated transmission protocols 1 to 4 are used as transmission control procedures on the A1SJ71C24-R2 and a no-protocol mode and a bidirectional mode are also available. The user can select and set these.

When using a dedicated transmission protocol or the no-protocol mode/bidirectional mode, data is transmitted using the codes as shown below.

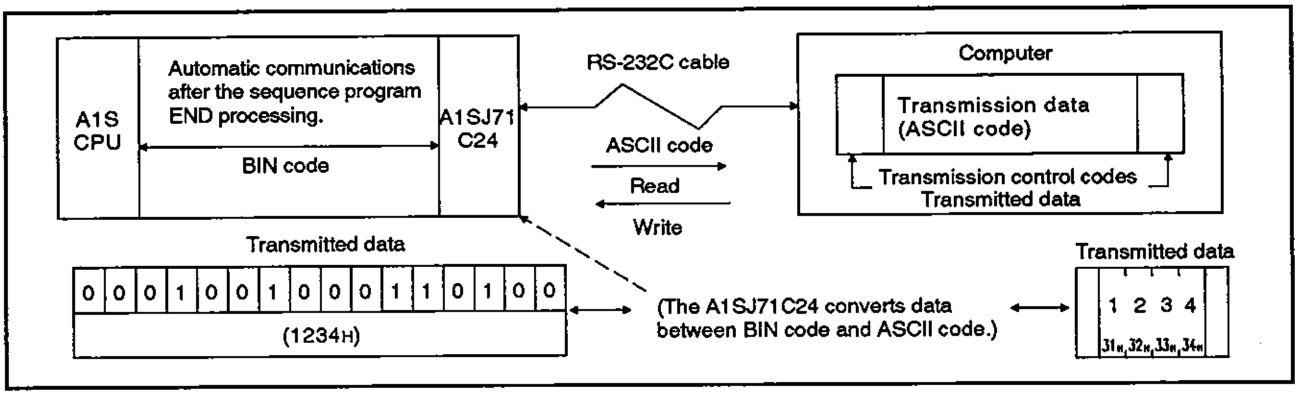


Fig. 1.1 Data Transmission with the Dedicated Protocol

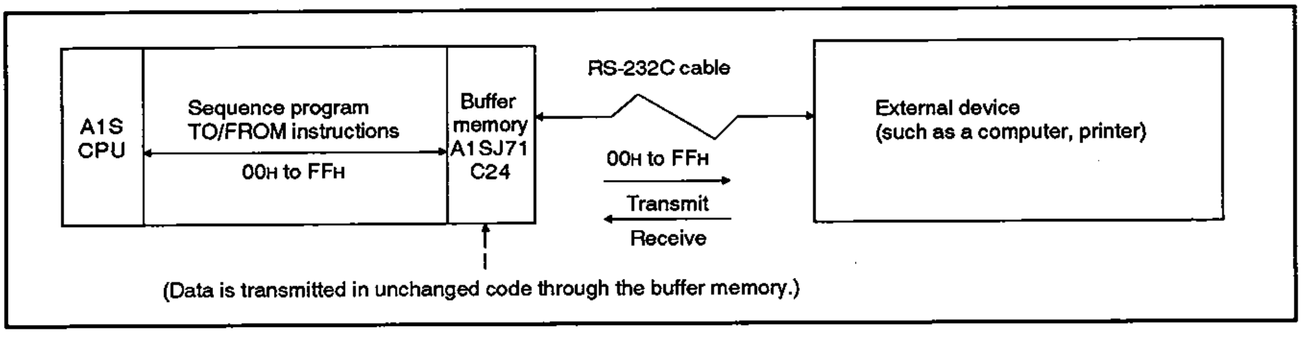


Fig. 1.2. Data Transmission in the No-Protocol Mode/Bidirectional Mode

1.1 Features

The features of the A1SJ71C24-R2 computer link module and the A1SJ71C24-PRF computer link/printer function module are given below.

1.1.1 Control operations in data communications

Data transmission operations between an A1SJ71C24 and external devices (e. g., computers) can be controlled using either the dedicated protocols (*1) or in the no-protocol/bidirectional mode. These control operations can be selected using individual A1SJ71C24.

(1) *Communications using the dedicated protocols*

(a) Communications at the request of the computer

Data communications is always initiated by the computer.

Designated data is transmitted according to the request command transmitted from a computer to an A1SJ71C24.

It is not necessary to create and change special sequence programs in order to use an A1SJ71C24.

1) Read and write possible to and from all PC CPU devices

Data can be read from all PC CPU devices. This permits observation and monitoring of all operations, as well as the collection and analysis of data. Data can be written to all PC CPU devices. This permits production control and production directives to be carried out.

2) An A1SJ71C24 can upload and download programs from a PC CPU.

PC CPU programs (main sequence and subsequence control programs and microcomputer programs), parameter data and comment data are read by the computer and stored. When required they can be written to the PC CPU to change the program.

3) Remote RUN and STOP control of the PC CPU

The PC CPU can be remote-controlled by means of RUN and STOP instructions from the computer.

4) When multiple computers and PC CPU modules are connected to a link with an A1SJ71C24 module, the input (X) signals of the CPUs in the link can be turned ON/OFF using any computer in the link. This function can immediately stop or simultaneously start all CPUs in the link.

(This function is called the global function of the A1SJ71C24.)

(b) Communications at the request of the PC CPU

The PC CPU transmits the data send request.

When the emergency data needs to be transmitted from a PC CPU to a computer, the PC CPU transmits a send request to the A1SJ71C24 to make the computer execute an interrupt processing.

(This is the on-demand function of the A1SJ71C24.)

* 1: The dedicated protocols consist of four different protocols. The term "dedicated protocols" used in this manual is the collective term for these protocols.

(2) Communications in the no-protocol/bidirectional modes

Either the no-protocol mode or the bidirectional mode can be set.

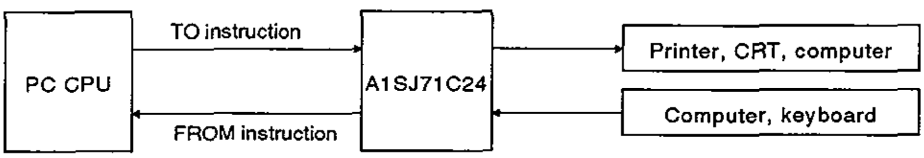
(a) Communications in the no-protocol mode

1) Data communications can be initiated by a PC CPU

Data communications can be initiated by a computer or any PC CPU. Data can be transmitted from a PC CPU to an external device by using the TO instruction in the sequence program to write data to the buffer memory.

Data transmitted from an external device can be read by a PC CPU using the FROM instruction in the sequence program.

The following example shows a system with a printer, CRT and keyboard terminal connected. Data can be output from the buffer memory to the printer or a CRT display using the TO instruction. Data input from the keyboard to the buffer memory can be read using a FROM instruction from the PC CPU.



2) Receiving data length can be set to variable or fixed:

The length of the data transmitted from an external device and received by the PC CPU can be set to variable or fixed.

i) Receiving variable-length data:

Data receive stops when the receive completed code set by the user is received.

ii) Receiving fixed-length data:

Data receive stops when the fixed length of data set by the user is received.

Both the receive completed code and the receive-completion data length can be freely set by the user.

3) Variable communications memory area

The user memory area can be allocated to suit the purpose and application of the data transmission.

(b) Bidirectional communications

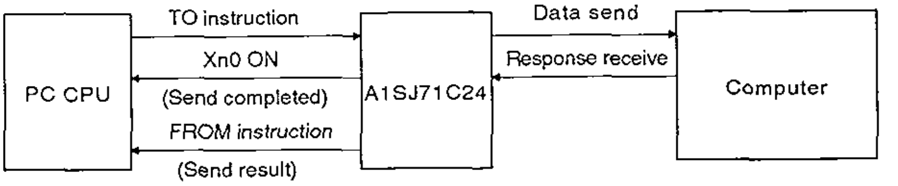
1) Data communications can be initiated by a PC CPU

Data communications can be initiated by a computer or any PC CPU. Data can be transmitted from a PC CPU to an external device by using the TO instruction in the sequence program to write data to the buffer memory.

The data send operation is completed when the response message to the sent (received) data is received from the computer. The result of the send (normal end/error) is stored in the buffer memory and can be read out.

The data received from the computer can be read with the FROM instruction of the sequence program.

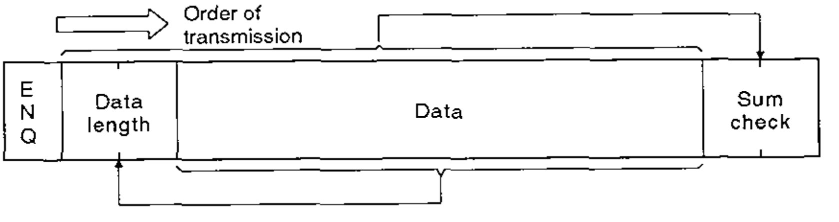
(When data is transmitted by an A1SJ71C24)



2) Data length is set within the send message

Data length is set within the send message when the data is transmitted to a device.

The receiving side recognizes the data length by the send message.



The send data of the A1SJ71C24 is processed as follows.

ENQ:.................... Added to the head.

Data length:........ The send data length set in the buffermemory is transmitted.

Data:.................... The send data stored in the buffer memoryis transmitted.

Sum check:......... Computed with the sum checking range in a message.

The data transmitted by a computer and received by an A1SJ71C24 is processed as follows.

ENQ:.................... Checked and removed from the received data.

Data length:........ Stored in the buffer memory as the received data length.

Data:.................... Stored in the buffer memory as the received data.

Sum check:......... Checked and removed from the received data.

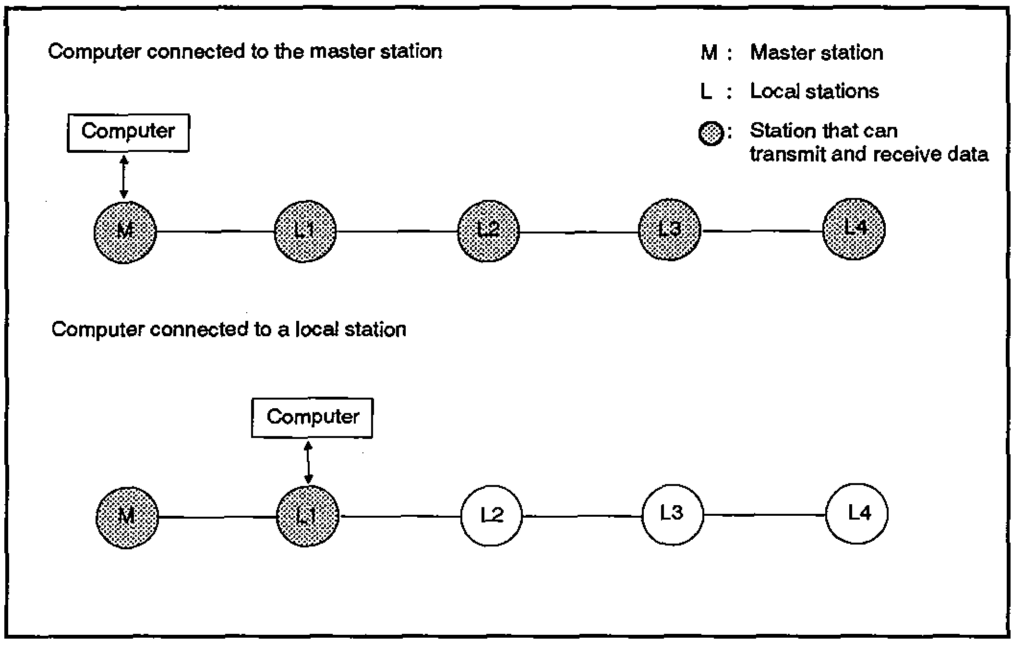
3) Variable communications memory area

The user memory area can be allocated to suit the purposes and applications of the data transmission.

1.1.2 Link with a computer through MELSECNET/B

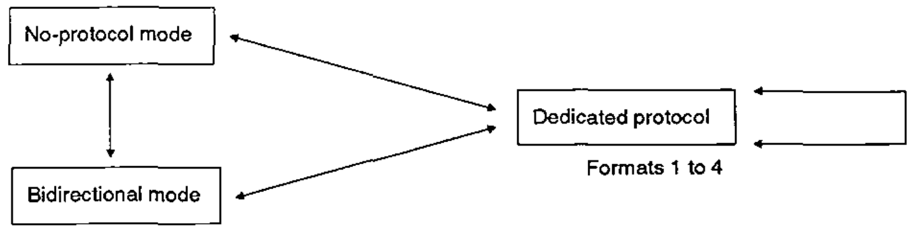
In a system connected through MELSECNET/B, if the system contains a PC CPU connected to a computer via an A1SJ71C24, data communications is possible between the computer and a PC CPU not equipped with the A1SJ71C24.

All data can be transmitted and received between a MELSECNET/B master station and local stations.



1.1.3 Mode switching function

The communications mode can be changed on line as shown below:



Use either of the following methods to change the mode:

- From an external device
- From a PC CPU

POINT

When the mode is changed from the dedicated protocol to the no-protocol or bidirectional mode, communications is done in the state of default value.

When communications is done using other than a default value, write necessary data to the special-purpose area before communicating with an external device.

1.1.4 Transmission control function

(1) Communications can be controlled using the DC code.

- The DC1/DC3 control is a function for notifying the communicating station of data transmission/receive enabled or disabled states using the DC1 and DC3.
- The DC2/DC4 control is a function for indicating the valid range of transmission/receive data using the DC2 and DC4.
- When data is transmitted or received, add the DC2 to the header and the DC4 to the end to transmit or receive data.

DC2	Data	DC4

(2) DTR control can be done.

- The DTR control is a function for notifying the communicating station of the data communications enabled or disabled status using the DSR/DTR signal.
- The A1SJ71C24 controls the DTR signal as follows:

  When data can be received: the A1SJ71C24 turns the DTR signal ON.

  When data cannot be received: the A1SJ71C24 turns the DTR signal OFF.
- The A1SJ71C24 controls transmission as follows according to the state of the DSR signal:

  When the DSR signal is ON: If there is send data, the A1SJ71C24 controls send data.

  When the DSR signal is OFF: Even if there is send data, the A1SJ71C24 does not transmit data until the DSR signal is turned ON.

1.1.5 Printer functions (for AJ71C24-PRF only)

Messages are registered from a computer or the PC CPU and output to a printer.

(1) Registering and reading a message

(a) Fixed messages up to 80 characters per message can be registered and read by using a computer with a CI (for registering) command (dedicated protocol) and a CJ (for reading) command.

(b) Fixed/free messages up to 80 characters per message can be registered and read by using the PC CPU with a TO (for registering) instruction and a FROM (for reading) instruction.

(2) Number of messages

Free messages can be registered up to 31 messages, and fixed messages, up to 400 messages.

(3) Printer output

Free and fixed messages for requested quantity of data can be output to a printer by making an output request from the PC CPU.

(4) Test output

Registered fixed messages or ASCII codes (21H to 7EH) can be output to a printer.

1.2 A1SJ71C24 Package

Open the package and make sure that it contains the following items:

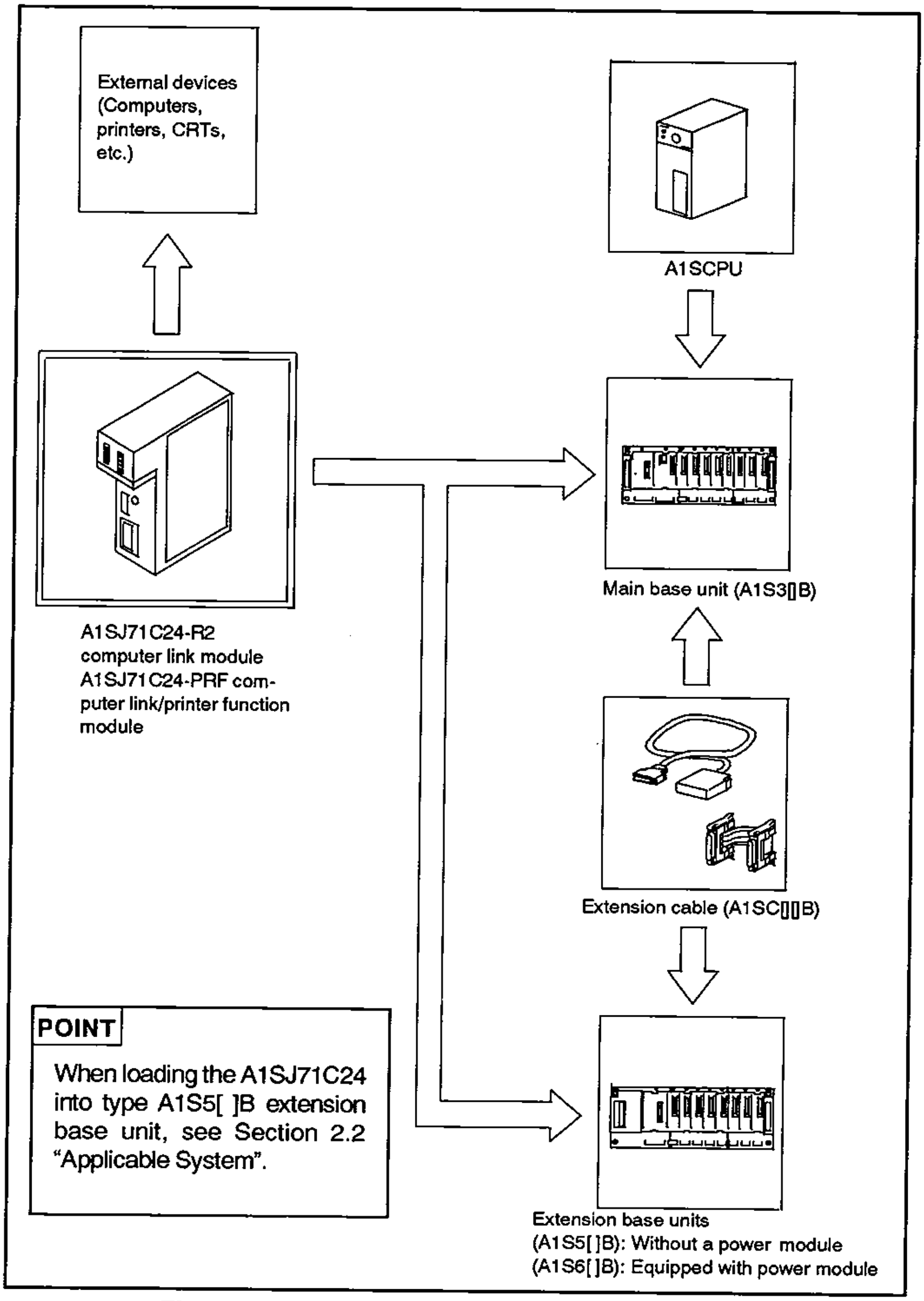
Item	Model (Type)	Number of Units
Link module	A1SJ71C24-R2 or A1SJ71C24-PRF	1
Connector	DDK 17JE-23090-02(D8A) (9-Pin D sub screw-holding type)	1

2. SYSTEM CONFIGURATIONS

This section describes system configurations which can be combined with the A1SJ71C24.

2.1 Overall Configurations

Fig. 2.1 shows the overall configuration of the A series system which is loaded with the A1SJ71C24.



POINT

When loading the A1SJ71C24 into type A1S5[ ]B extension base unit, see Section 2.2 "Applicable System".

Fig. 2.1 A Series System Overall Configuration

2.2 Applicable Systems

The A1SJ71C24 can only be used in the systems described below.

(1) Applicable PC CPU modules and the number of A1SJ71C24 modules

PC CPU Modules	Number of Connectable A1SJ71C24s	Notes
A1S	2	If the following modules are used with an A1SJ71C24 when A-series extension base units (A5[ ]B or A6[ ]B) are used, the maximum number of connectable A1SJ71C24 modules cannot exceed 2. (See previous column). • AD51(S3)/AD51H Intelligent Communication Module • AD57G Graphic controller module • AJ71C21(S1) Terminal Interface Module • AJ71C22(S1) Multidrop Link System Module • AJ71C23 Higher Controller High Speed Link Module • AJ71C24(S3/S6/S8) Computer Link Module • AJ71E71 Ethernet Interface Module

(2) Applicable base unit

The A1SJ71C24 can be inserted into any slot of a main base unit or extension base unit with these two exceptions:

The power supply capacity may be insufficient to load the A1SJ71C24 into an extension base unit with no built-in power supply (A1S5[ ]B or A5[ ]B). Wherever possible, avoid loading an A1SJ71C24 module into this type of extension base unit. If it is necessary to use an A1SJ71C24 module in an extension base unit with no built-in power supply, it is important to consider (a) the power supply capacity of the main base unit, and (b) the voltage drop along the extension cables when selecting the extension cables.

(The User's Manual of A1SCPU module employed gives details.)

2.3 System Configurations of computer link and Available Functions

The A1SJ71C24 is a link module to connect an external device (such as a computer) and a PC CPU. The connection may be made in one way: using the RS-232C port.

2.3.1 The system configuration an external device (computer) to a PC CPU

(1) The system configuration for an external device (such as a computer) to a PC CPU is shown in Fig. 2.2 below.

(Mode: [ ] – [ ]) in the figure indicates the range of setting set with the mode setting switch of an A1SJ71C24 (see Section 4.3.1).

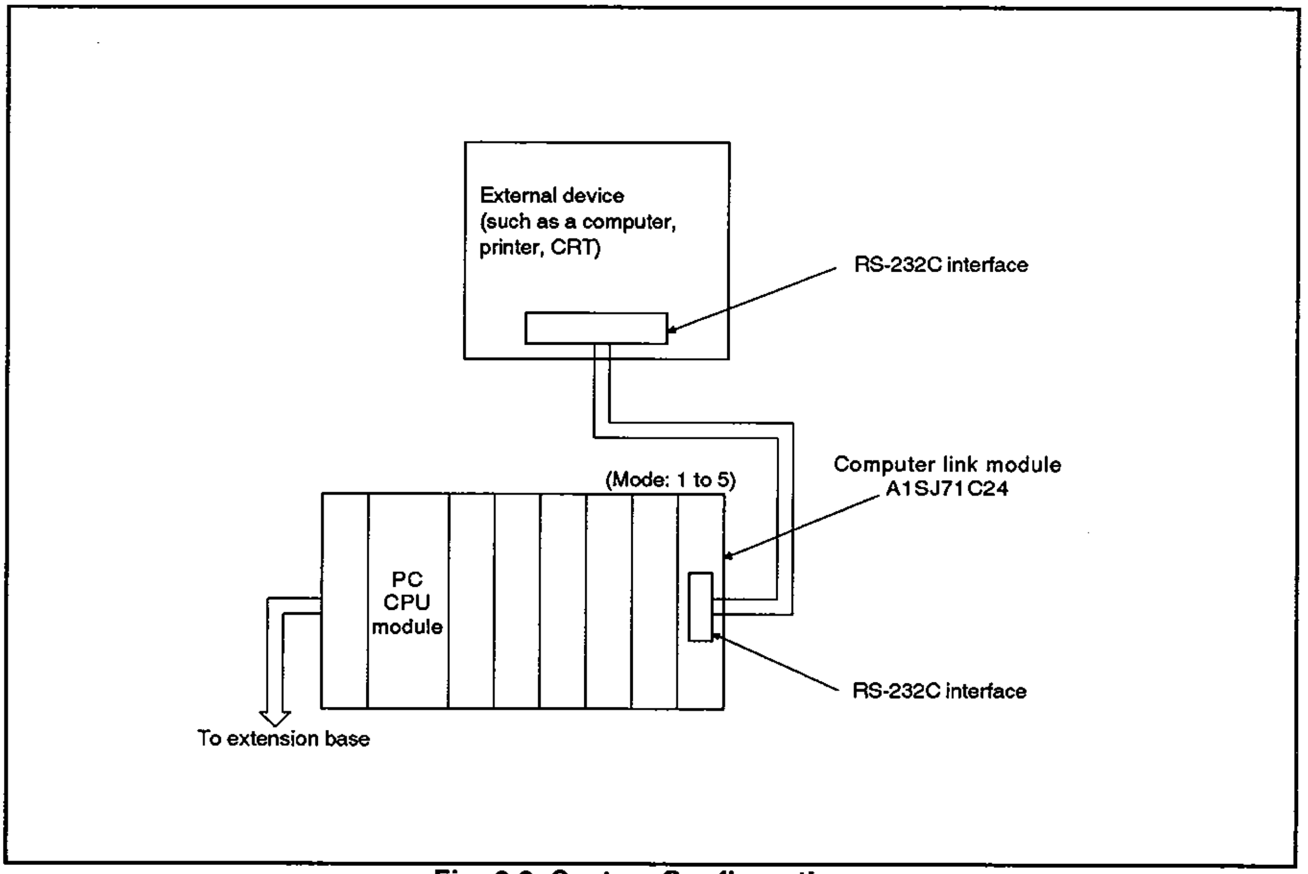


Fig. 2.2 System Configurations

(2) The following tables list the functions available when an external device is linked with a PC CPU module to make a 1 : 1 configuration.

(a) The interface used to set dedicated protocols 1 to 4:

1) *Functions available when using an external device*

Available Functions		Interfaces for Dedicated Protocol	Note
Device memory	Read/write	o	—
	Test		
	Monitor		
Extension file registe	Read/write	o	
	Test		
	Monitor		
Buffer memory A1SJ71C24 of the self	Read/write	o	
Special function module's buffer memory	Read/write	o	
Sequence/ Microcomputer program	Read/write	o	
Comment	Read/write	o	
Parameter	Read/write	o	
PC CPU	Remote RUN/STOP	o	
	PC CPU type read	o	
Global	Input signal (X) ON/OFF	o	
Self-loopback test	Transmission of received data	o	

2) Functions available when using a PC CPU

Available Functions		Interfaces for Dedicated Protocol	Note
On-demand	Data transmission to external devices	o	–

(b) Interfaces used to set the no-protocol mode

Functions available when using an external device and a PC CPU

Available Functions		Interfaces for No- Protocol Mode	Note
Send	PC CPU to external device	o	To computers, printers, and CRTs.
Receive	External device to PC CPU	o	From computers and keyboards

(c) Interfaces used to set the bidirectional mode

Functions available when using an external device and a PC CPU

Available Functions		Interfaces for Bidirectional Mode	Note
Send	PC CPU to computer	o	To computers
Receive	Computer to PC CPU	o	From computers

2.3.2 System configurations when A1SJ71C24s are used with external devices (such as computer) by connecting the A1SJ71C24s to the PC CPUs in a MELSECNET/B system.

By loading A1SJ71C24s to the PC CPUs in a MELSECNET/B, communications can be done with the PC CPU of another station.

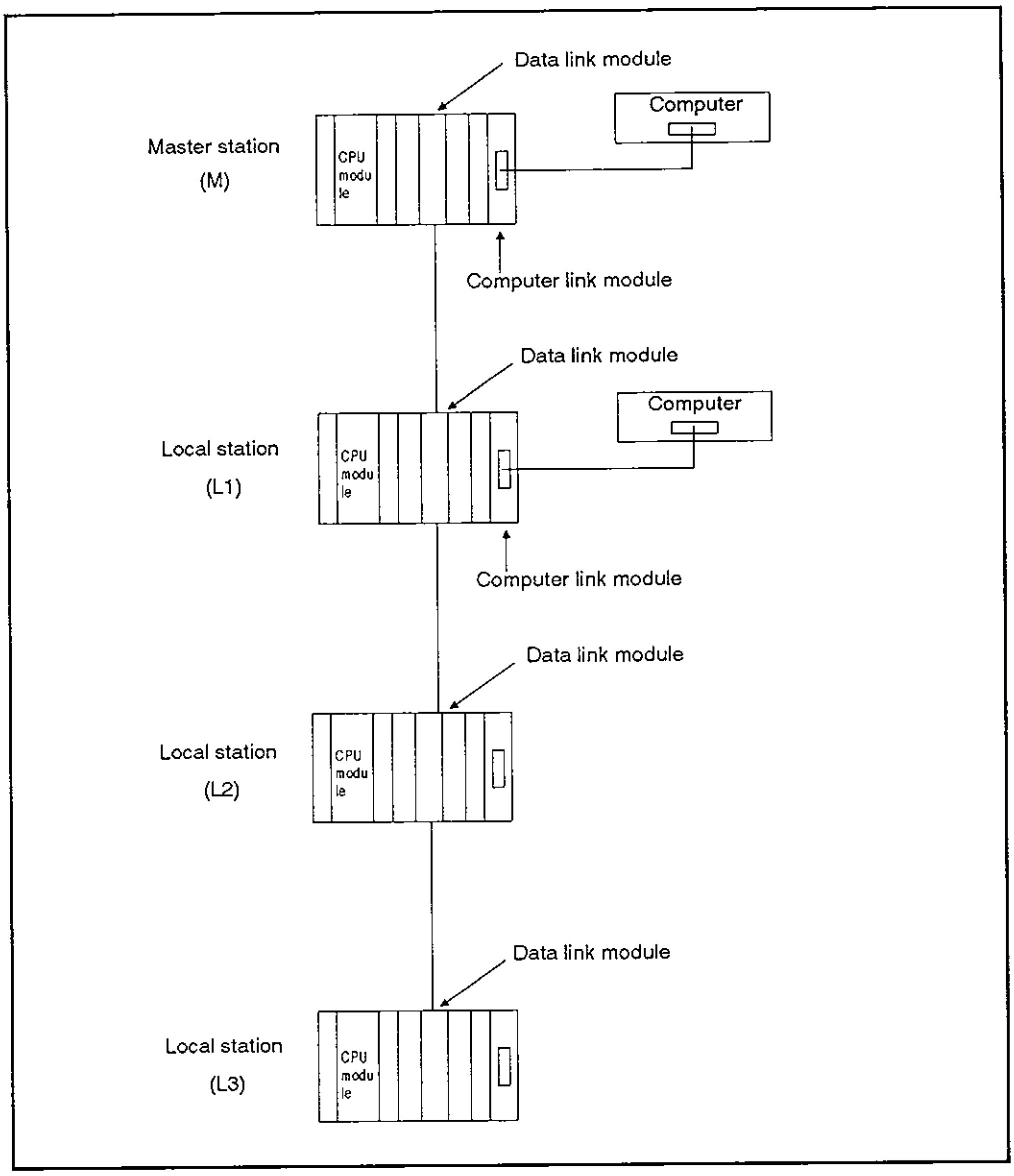


Fig. 2.3 System Configuration (11)

The PC CPUs that can be communicated with:

(PC CPUs to which A1SJ71C24s are connected) (MELSECNET/B stations that can be communicated with)

* M station (Master station)	: (1) Self station
	(2) All 2-tier local stations (L1, L2, L3)
* L station (Local station)	: (1) Self station
	(2) Master station (M station)

2.4 Functions Available When Using the System Configurations of Printer Functions

This section explains the system configurations applied when the A1SJ71C24-PRF printer functions are used.

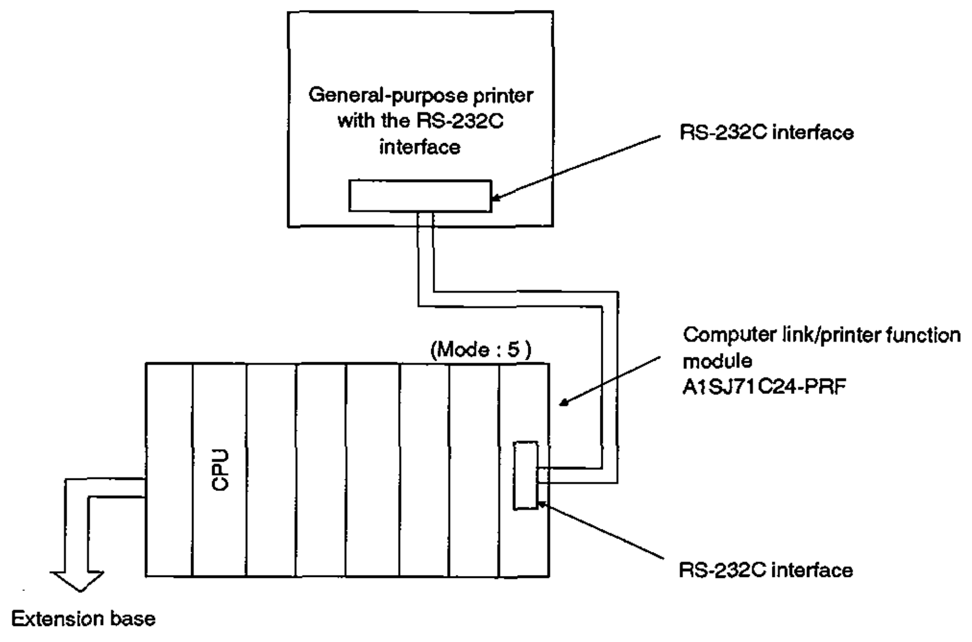
The RS-232C interface is used for connecting a printer to a PC CPU.

2.4.1 System configurations when a printer is linked with a PC CPU

(1) The system configuration for a 1 : 1 ratio of a printer to a PC CPU is shown in Fig. 2.4 below.

The (Mode: [ ] to [ ]) in the figure below shows the range of the set value of the mode setting switch (Section 4.3) of the station.

1:1



POINTS

(1) The printer functions can be used only with an A1SJ71C24-PRF.

(2) When using the printer functions, designate the function at the printer function designation area (800H) of the buffer of the A1SJ71C24-PRF.

Fig. 2.4 System Configurations (III)

(2) The following A1SJ71C24-PRF functions can be used with the system configurations when a printer is linked with a PC CPU.

(a) Functions that can be used from a PC CPU

Function	Content	RS-232C
Registration/ read of a printer message with a sequence program	Fixed/free messages of up to 80 characters can be registered/read with a sequence program.	O
Printer output function	Fixed/free messages can be registered/ read by making a printer output request from a sequence program.	O
Printer test output function	The following two kinds of test outputs are enabled by making a printer output request from a sequence program: (1) Contents of a registered fixed message are output to the printer. (2) ASCII codes (21H to 7EH) are output to the printer.	O

(b) Function that can be used from a computer

Function	Contents	RS-232C
Registration/ read of a printer message from a computer	A fixed message of up to 80 characters can be registered/read by using a CI (fixed message data registration) or CJ (fixed message data read) command of dedicated protocol 1 to 4 (mode 1 to 4).	X

3. SPECIFICATIONS

3.1 General Specifications

Table 3.1 General Specifications

Item	Specifications				
Operating ambient temperature	0 to 55°C (32 to 131°F)				
Storage ambient temperature	–20 to 75° (4 to 167°F)				
Operating ambient humidity	10 to 90% RH, no condensation				
Storage ambient humidity	10 to 90% RH, no condensation				
Vibration resistance	Conforms to **JIS C 0911	Frequency	Acceleration	Amplitude	Sweep Count
		10 to 55 Hz	—	0.075 mm (0.003 inch)	10 times *(1 octave/ minute)
		55 to 150 Hz	9.8 m/s^2 (1 g)	—	
Shock resistance	Conforms to JIS C 0912 (98 m/s^2(10g) x 3 times in 3 directions)				
Noise resistance	By noise simulator 1500 V.P.P. noise voltage, 1 μsec noise width and 25 to 60 Hz noise frequency				
Dielectric withstand voltage	1500 VAC for 1 minute across AC external terminals and ground 500 VAC for 1 minute across DC external terminals and ground				
Insulation resistance	5 MΩ or greater by 500 VDC insulation resistance tester across AC external terminals and ground				
Grounding	Class C grounding when necessary. If grounding is impossible, make grounding to the panel.				
Operating ambience	No corrosive gases or dust.				
Cooling method	Self-cooling				

REMARK

One octave marked * indicates a change from the initial frequency to double or half frequency. For example, any of the changes from 10 Hz to 20 Hz, 20 Hz to 40 Hz, 40 Hz to 20 Hz, and 20 Hz to 10 Hz are referred to as one octave.

** JIS: Japanese Industrial Standard

3.2 Performance Specifications

3.2.1 Transmission specifications

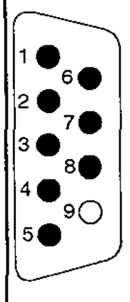
Table 3.2 Transmission Specifications

Item		Specifications	
Interface		Conform to RS-232C.	
Transmission method		Dedicated protocol	Half-duplex communications system *1
		No-protocol/bidirectional/printer function	Full-/half-duplex (buffer memory setting)
Synchronous system		Asynchronous system	
Transmission system		300, 600, 1200, 2400, 4800, 9600, 19200 BPS (switch selected)	
Data format	Start bit	1	
	Data bit	7 or 8	Selectable
	Parity bit	1 or none	
	Stop bit	1 or 2	
Access cycle		Each request is processed in the END processing of the sequence program. Therefore, access cycle is 1 scan time.	
Error detection		Parity check present (odd/even)/absent	
		Sum check present/absent	
DTR/DSR (ER/DR) control		YES/NO (Select either by using the buffer)	
X ON/OFF (DC1/DC3) control			
System configuration (External device: PC CPU)		Dedicated protocol	1 : 1
		No-protocol/printer function	1 : 1
		Bidirectional	1 : 1
Transmission distance		Up to 15 m (49.2 ft) for RS-232C	
Current consumption		5 VDC, 0.1 A	
Number of occupying I/Os		32 *2	
Weight		220g (0.49 lb)	
Recommended RS-232C to RS-422 converter		EL-LINE-M	

*1: If the on-demand function is used, only full-duplex communications is available when full-duplex communications is enabled.

*2: Set the special function modules to have 32 inputs/outputs when the I/O allocation is set.

3.2.2 RS-232C connector specifications



Pin Number	Signal Abbreviation	Signal Name	Signal Direction A1SJ71C24↔External Device
1	CD	Receive carrier detection	←
2	RD(RXD)	Receive data	←
3	SD(TXD)	Send data	→
4	DTR(ER)	Data terminal ready	→
5	SG	Signal ground	↔
6	DSR(DR)	Data set ready	←
7	RS(RTS)	Request to send	→
8	CS(CTS)	Clear to send	←

Fig. 3.1 RS-232C Connector Specifications

(1) Signals are described below.

(a) CD signal

The A1SJ71C24 operates according to the setting of the CD terminal check.

	CD Terminal Check Enabled	CD Terminal Check Disabled
Full-duplex	The A1SJ71C24 performs transmission processing when the CD signal (receive carrier detection) is ON. The transmission sequence of the A1SJ71C24 is initialized when the CD signal is turned OFF during data communications in the dedicated protocol.	The A1SJ71C24 performs transmission processing regardless of the ON/OFF state of the CD signal. (This enables data communications with those external devices which cannot control (ON/OFF) the CD signal.)
Half-duplex	See Section 5.	Setting impossible

(b) DTR signal

The A1SJ71C24 system controls the DTR signal as follows:

The A1SJ71C24 system turns ON the DTR signal when communications is enabled if the dedicated protocol is currently used.

The A1SJ71C24 system turns ON/OFF the DTR signal according to the size of available area of the receive data storage OS area during communications in the no-protocol mode. (The DTR signal turns ON when the data communications of the A1SJ71C24 is enabled.)

Appendix 4 gives for the ON/OFF timing of the DTR signal when using the no-protocol mode.

Since the received data is stored in the OS area when the DTR signal is OFF, read the received data using the sequence program (See Section 9).

POINT

When the printer function is used, operations are same as those in no-protocol mode.

(c) SG signal

Connect the shield of the connecting cable to pin 5 of the A1SJ71C24.

(d) DSR signal

Data is only transmitted from the A1SJ71C24 when this signal is ON.

(e) RS signal

The A1SJ71C24 system turns ON/OFF the RS signal according to the setting of the CD terminal check (see Section 7.1) and the transmission method (see Section 7.2), as shown below.

Transmission Method	CD terminal Check Setting	State of the CD Signal	RS Signal ON/OFF Control
Full-duplex	Enabled	ON	When the A1SJ71C24 is in the ready state, the A1SJ71C24 system turns RS signal ON.
		OFF	The A1SJ71C24 system turns the RS signal OFF.
	Disabled	ON	When the A1SJ71C24 is in the ready state, the A1SJ71C24 system turns the RS signal ON. (normally ON)
		OFF	
Half-duplex	Enabled (always set to enabled)	ON	See Section 5.
		OFF	

Data transmission from the external device should be done confirming the RS signal controlled by the A1SJ71C24.

(f) CS signal

Data is only transmitted from the A1SJ71C24 when this signal is ON.

(2) ON/OFF definitions are as follows:

ON : 5V to 15 VDC

OFF : –5 V to –15 VDC

(3) Interface connector

The following type of RS-232C connector is used. Use a matching connector.

9-pin D-sub (female) screw-fixing type

3.3 Functions List

The tables below list the functions available when an external device (such as a computer) and a PC CPU are connected by an A1SJ71C24 module.

3.3.1 Computer link functions

(1) Functions available using dedicated protocols and commands

The functions available using dedicated protocols 1 to 4 are listed in Tables 3.3 and 3.4.

The commands in Table 3.3 can be used for an A1SCPU connected to the A1SJ71C24 or for the ACPU of another station.

The commands in Table 3.4 can be used for an A2ACPU(P21/R21)(S1) or A3ACPU(P21/R21) over the data link.

(a) Functions available with the ACPU common commands

Table 3.3 Functions List When Using a Dedicated Protocol

<table>
<tr><th colspan="3" rowspan="2">Function</th><th colspan="2">Command</th><th rowspan="2">Description</th><th rowspan="2">Number of Point Processed per Communications</th></tr>
<tr><th>Sym-bol</th><th>ASCII Code</th></tr>
<tr><td rowspan="14">Device memory</td><td rowspan="3">Batch read</td><td>Bit units</td><td>BR</td><td>42H, 52H</td><td>Reads bit devices (such as X, Y, M) in units of 1 device.</td><td>256 points</td></tr>
<tr><td rowspan="2">Word units</td><td rowspan="2">WR</td><td rowspan="2">57H, 52H</td><td>Reads bit devices (such as X, Y, M) in units of 16 devices.</td><td>32 words (512 points)</td></tr>
<tr><td>Reads word devices (such as D, R, T, C) in units of 1 device.</td><td>64 points</td></tr>
<tr><td rowspan="3">Batch write</td><td>Bit units</td><td>BW</td><td>42H, 57H</td><td>Writes bit devices (such as X, Y, M) in units of 1 device.</td><td>160 points</td></tr>
<tr><td rowspan="2">Word units</td><td rowspan="2">WW</td><td rowspan="2">57H, 57H</td><td>Writes bit devices (such as X, Y, M) in units of 16 devices.</td><td>10 words (160 points)</td></tr>
<tr><td>Writes word devices (such as D, R, T, C) in units of 1 device.</td><td>64 points</td></tr>
<tr><td rowspan="3">Test (ran-dom write)</td><td>Bit units</td><td>BT</td><td>42H, 54H</td><td>Specifies bit devices (such as X, Y, M) and device number in units of 1 device at random and sets/resets the device.</td><td>20 points</td></tr>
<tr><td rowspan="2">Word units</td><td rowspan="2">WT</td><td rowspan="2">57H, 54H</td><td>Specifies bit devices (such as X, Y, M) and device number in units of 16 devices at random and sets/resets the device.</td><td>10 words (160 points)</td></tr>
<tr><td>Specifies word devices (such as D, R, T, C) and device number in units of 1device at random and sets/resets the device.</td><td>10 points</td></tr>
<tr><td rowspan="3">Monitor data entry</td><td>Bit units</td><td>BM</td><td>42H, 4DH</td><td>Sets bit devices to be monitored (such as X, Y, M) in units of 1 device.</td><td>40 points *1</td></tr>
<tr><td rowspan="2">Word units</td><td rowspan="2">WM</td><td rowspan="2">57H, 4DH</td><td>Sets bit devices to be monitored (such as X, Y, M) in units of 16 devices.</td><td>20 words *1 (320 points)</td></tr>
<tr><td>Sets word devices to be monitored (such as D, R, T, C) in units of 1 device.</td><td>20 points</td></tr>
<tr><td rowspan="2">Monitor</td><td>Bit units</td><td>MB</td><td>4DH, 42H</td><td rowspan="2">Reads data from devices for which device data registration has been made.</td><td rowspan="2">—</td></tr>
<tr><td>Word units</td><td>MN</td><td>4DH, 4EH</td></tr>
<tr><td rowspan="5">Extension file register</td><td colspan="2">Batch read</td><td>ER</td><td>45H, 52H</td><td>Reads extension file registers (R) in units of 1 register.</td><td>64 points</td></tr>
<tr><td colspan="2">Batch write</td><td>EW</td><td>45H, 57H</td><td>Writes extension file registers (R) in units of 1 register.</td><td>64 points</td></tr>
<tr><td colspan="2">Test (random write)</td><td>ET</td><td>45H, 54H</td><td>Specifies the extension file registers (R) in units of 1 register using block or device number and makes a random write.</td><td>10 points</td></tr>
<tr><td colspan="2">Monitor data registration</td><td>EM</td><td>45H, 4DH</td><td>Sets the extension file registers (R) device numbers to be monitored in units of 1 register.</td><td>20 points</td></tr>
<tr><td colspan="2">Monitor</td><td>ME</td><td>4DH, 45H</td><td>Monitors the extension file register after monitor data registration.</td><td>—</td></tr>
</table>

PC CPUs with which the Command can be Executed											PC CPU State			Reference Section
	PC CPUs of the Communicating Stations over the Data Dink											During RUN		
A1S	A1S	A0J 2H	A1N A1	A2N A2 (S1)	A2A (S1)	A3N A3	A3A	A3H	A3M	A73	During STOP	SW04 ON	SW04 OFF	
o	o										o	o	o	8.7.2 8.7.3
o	o										o	o	x	8.7.4 8.7.5
o	o										o	o	x	8.7.6 8.7.7
o	o										o	o	o	8.7.8
o	o										o	o	o	
o	o		x	o							o	o	o	8.8.4
o	o		x	o							o	o	x	8.8.5
o	o		x	o							o	o	x	8.8.8
o	o		x	o							o	o	o	8.8.9
o	o		x	o							o	o	o	

Table 3.3 Functions List When Using a Dedicated Protocol (Continued)

Function				Command Symbol	Command ASCII Code	Description		Number of Point Processed per Communications
Buffer memory	Batch read			CR	43H, 52H	Reads data from the A1SJ71C24 buffer memory.	Also usable for communications between the sequence program and the external devices when a multi-drop link is made.	64 words (128 bytes)
	Batch write			CW	43H, 57H	Writes data to the A1SJ71C24 buffer memory.		
Special function module	Batch read			TR	54H, 52H	Reads the contents of the special function module buffer memory.		64 words (128 bytes)
	Batch write			TW	54H, 57H	Writes data to the special function module buffer memory.		
Sequence Program	Batch read	Main	Other than T/C set value	MR	4DH, 52H	Reads main sequence programs.		64 steps
			T/C set value			Reads T/C set values used in main sequence programs.		64 points
		Sub	Other than T/C set value	SR	53H, 52H	Reads subsequence programs.		64 steps
			T/C set value			Reads T/C set values used in subsequence programs.		64 points
	Batch write	Main	Other than T/C set value	MW	4DH, 57H	Writes main sequence programs.		64 steps
			T/C set value			Writes T/C set values used in main sequence programs.		64 points
		Sub	Other than T/C set value	SW	53H, 57H	Writes subsequence programs.		64 steps
			T/C set value			Writes T/C set values used in subsequence programs.		64 points
Micro computer program	Batch read		Main	UR	55H, 52H	Reads main microcomputer programs.		128 bytes
			Sub	VR	56H, 52H	Reads submicrocomputer programs.		
	Batch write		Main	UW	55H, 57H	Writes main microcomputer programs.		
			Sun	VW	56H, 57H	Writes submicrocomputer programs.		
Comment	Batch read			KR	4BH, 52H	Reads comment data.		128 bytes
	Batch write			KW	4BH, 57H	Writes comment data.		
Parameter	Batch read			PR	50H, 52H	Reads parameters from PC CPU.		128 bytes
	Batch write			PW	50H, 57H	Writes parameters to PC CPU.		
	Analysis request			PS	50H, 53H	Causes PC CPU to acknowledge and check rewritten parameters.		—
PC CPU	Remote RUN			RR	52H, 52H	Request remote run/stop of PC CPU.		—
	Remote STOP			RS	52H, 53H			
	PC CPU read			PC	50H, 43H	Reads the type of PC CPU: A1N, A2N, A3N, A3H		
Global				GW	47H, 57H	Turns ON and OFF the global signal of the A1SJ71C24 loaded in each PC CPU system.		1 point
On-demand				—		Send request is initiated by a PC CPU. (Available in a 1:1 ratio system.)		Data length specified in the sequence program. (Max. 1760 words)
Loopback test				TT	54H, 54H	Echoes unchanged characters back to the computer.		254 characters

<table>
<tr><th colspan="11">PC CPUs with Which the Command can be Executed</th><th colspan="3" rowspan="2">PC CPU State</th><th rowspan="4">Reference Sections</th></tr>
<tr><th rowspan="3">A1S</th><th colspan="10">PC CPUs of the Communicating Stations over the Data Link</th></tr>
<tr><th rowspan="2">A1S</th><th rowspan="2">A0J
2H</th><th rowspan="2">A1N
A1</th><th rowspan="2">A2N
A2 (S1)</th><th rowspan="2">A2A
(S1)</th><th rowspan="2">A3N
A3</th><th rowspan="2">A3A</th><th rowspan="2">A3H</th><th rowspan="2">A3M</th><th rowspan="2">A73</th><th rowspan="2">During STOP</th><th colspan="2">During RUN</th></tr>
<tr><th>SW04 ON</th><th>SW04 OFF</th></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td>8.9.2
8.9.3</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td>8.10.3</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>x</td><td>8.10.3</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td rowspan="6">8.12.4</td></tr>
<tr><td>x</td><td colspan="5">x</td><td colspan="5">o</td><td>o</td><td>o</td><td>o</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o *2</td><td>x</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>x</td></tr>
<tr><td>x</td><td colspan="5">x</td><td colspan="5">o</td><td>o</td><td>o</td><td>x</td></tr>
<tr><td>x</td><td colspan="5">x</td><td colspan="5">o</td><td>o</td><td>o *2</td><td>x</td></tr>
<tr><td>o</td><td colspan="4">o</td><td rowspan="2">x</td><td rowspan="2">o</td><td rowspan="2">x</td><td colspan="3" rowspan="2">o</td><td rowspan="2">o</td><td rowspan="2">o</td><td rowspan="2">o</td><td rowspan="4">8.12.5</td></tr>
<tr><td>x</td><td colspan="4">x</td></tr>
<tr><td>o</td><td colspan="4">o</td><td rowspan="2">x</td><td rowspan="2">o</td><td rowspan="2">x</td><td colspan="3" rowspan="2">o</td><td rowspan="2">o</td><td rowspan="2">o *2</td><td rowspan="2">x</td></tr>
<tr><td>x</td><td colspan="4">x</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td rowspan="2">8.12.6</td></tr>
<tr><td>x</td><td colspan="10">o</td><td>o</td><td>o</td><td>x</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td rowspan="3">8.12.3</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>x</td><td>x</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>x</td><td>x</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td>8.11.2</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td>8.11.3</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td>8.13</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>–</td><td>o</td><td>o</td><td>8.14</td></tr>
<tr><td>o</td><td colspan="10">o</td><td>o</td><td>o</td><td>o</td><td>8.15</td></tr>
</table>

*1: When the CPU modules other than A3H, A2A(S1), and A3A are used, devices X (input) are allocated with 2 inputs per device.

To include devices X in designated devices, set as follows:

((number of designated X devices x 2) + number of other designated devices) $\leq$ 40

If only devices X are designated, the number of inputs usable for one communications time is half the value mentioned in the table.

*2: Writing during a program run may be carried out if all the following conditions are met:

(This is different from the write during PC RUN with a MELSEC-A series peripheral device (e.g., A6GPP).)

(a) The PC CPU is type A3, A3N, A3H, A3M, A73 or A3A.

(b) The program is not the currently running program.

(includes subprograms called by the currently running main program)

(c) The PC CPU special relay is in the following states:

1) M9050 signal flow exchange contact ....OFF (A3CPU only)

2) M9051 (CHG instruction disable)...................ON

POINT

When the A1SJ71C24 is used together with the A2ACPU (S1) or A3ACPU, use the commands in Table 3.4 to perform the following functions:

- Batch read/write, test, monitor data registration, and monitor of device memory
- Batch read/write of extension file registers by designating device numbers (continuous numbers)
- Batch read/write of extension comments

When the commands in Table 3.3 are used, the available functions and the range of devices which can be designated are limited to those available with the A3HCPU.

Accordingly, A2ACPU(S1) and A3ACPU external devices are not accessible.

(b) Functions available with the AnACPU dedicated commands

Table 3.4 Functions List When Using a Dedicated Protocol

Function			Commands: Symbol	Commands: ASCII Code	Description	Number of Point Processed per Communications	PC CPU State: During STOP	PC CPU State: During RUN SW04 ON	PC CPU State: During RUN SW04 OFF	Reference Sections
Device memory	Batch read	Bit units	JR	4AH, 52H	Reads bit devices (such as X, Y, M) in units of 1 device.	256 points	o	o	o	8.7.2
		Word units	QR	51H, 52H	Reads bit devices (such as X, Y, M) in units of 16 devices.	32 words (512 points)				8.7.3
					Reads word devices (such as D, R, T, C) in units of 1 device.	64 points				
	Batch write	Bit units	JW	4AH, 57H	Writes bit devices (such as X, Y, M) in units of 1 device.	160 points	o	o	x	8.7.4
		Word units	QW	51H, 57H	Writes bit devices (such as X, Y, M) in units of 16 devices.	10 words (160 points)				8.7.5
					Writes word devices (such as D, R, T, C) in units of 1 device.	64 points				
	Test (random write)	Bit units	JT	4AH, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 1 device at random and sets/resets the device.	20 points	o	o	x	8.7.6
		Word units	QT	51H, 54H	Specifies bit devices (such as X, Y, M) and device number in units of 16 devices at random and sets/resets the device.	10 words (160 points)				8.7.7
					Specifies word devices (such as D, R, T, C) and device number in units of 1 device at random and sets/resets the device.	10 points				
	Monitor data registration	Bit units	JM	4AH, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 1 device.	40 points	o	o	o	8.7.8
		Word units	QM	51H, 4DH	Sets bit devices to be monitored (such as X, Y, M) in units of 16 devices.	20 words (320 points)				
					Sets word devices to be monitored (such as D, R, T, C) in units of 1 device.	20 points				
	Monitor	Bit units	MJ	4DH, 4AH	Reads data from devices for which device data has been registered.	—	o	o	o	
		Word units	MQ	4DH, 51H						
Extension file register	Direct read	Word units	NR	4EH, 52H	Reads data in units of 1 device by designating the device numbers continuously regardless of the extension file register block numbers.	64 points	o	o	o	8.8.6
	Direct write	Word units	NW	4EH, 57H	Writes data in units of 1 device by designating the device numbers continuously regardless of the extension file register block numbers.	64 points	o	o	x	8.8.7
Extension comment	Batch read		DR	44H, 52H	Reads the extension comment data.	128 bytes	o	o	o	8.12.7
	Batch write		DW	44H, 57H	Writes the extension comment data.		o	o	x	

POINT

The commands given in Table 3.4 can be used when the A1SJ71C24 is used together with the A2ACPU(S1) or A3ACPU. The whole range of device memory is accessible using these commands.

For functions other than those listed in Table 3.4, use the commands given in Table 3.3.

(2) Functions available in the no-protocol mode

(a) Functions in the no-protocol mode

Function	Command	Description	Number of Points Processed per Communications	PC CPU State			Reference Section
				During STOP	During RUN		
					SW04 ON	SW04 OFF	
Send (PC CPU → external device)	—	A PC CPU uses the TO instruction to output data written to an A1SJ71C24 buffer memory area in unchanged code to an external device.	127 words (default value). Can be changed with buffer size setting (see Sections 7.4.4 and 7.4.5.).	o	o	o	Section 9
Receive (External device → PC CPU)	—	A PC CPU uses the FROM instruction to read from an A1SJ71C24 buffer memory which was transmitted from an external device.					

(b) Receive completion by the completed code and by the completion data length

There are two ways to complete the data receive when an A1SJ71C24 is receiving data from an external device:

1) Reading the received data using the receive completed code (receive of variable-length data)

When an A1SJ71C24 receives the receive completed code which is set in the buffer memory by the user from an external device, the A1SJ71C24 transmits a received data read request to the sequence program.

The sequence program, in response to the read request, reads the received data up to the receive completed code transmitted by the external device.

The user can freely set the receive completed code.

2) Reading the received data using the receive-completion data length (receive of fixed-length data)

When an A1SJ71C24 receives data of a designated length which is set in the buffer memory by the user from an external device, the A1SJ71C24 transmits a received data read request to the sequence program.

The sequence program, in response to the read request, reads the received data of the designated length transmitted by the external device.

The receive-completion data length can be set within the buffer memory area allocated for the no-protocol receive.

POINTS

(1) The functions available with the no-protocol mode cannot be used together with the functions available with the bidirectional mode mentioned in Section 3.3.1.(3). Select either mode using the mode setting switch (see Section 4.3.1) and by setting the bidirectional mode setting area in the special applications buffer memory area (see Sections 3.5 and 10.2).

(2) The receive-completed code and the receive-completion data length can be set and enabled at the same time. When both of them are enabled, the received data read request to the sequence program is made in response to whichever is received first by the A1SJ71C24.

(3) Functions available in the bidirectional mode

(a) Functions in the bidirectional mode

Function	Command	Description	Number of Points Processed per Communications	PC CPU State			Reference Section
				During STOP	During RUN		
					SW04 ON	SW04 OFF	
Send (PC CPU → computer)	—	A PC CPU uses the TO instruction to output data written to the A1SJ71C24 buffer memory area in unchanged code to a computer. When the A1SJ71C24 receives the response message from a computer after data send the A1SJ71C24 transmits a send completed signal to the sequence program.	127 words (default value). Can be changed with the buffer size setting (see Sections 7.4.4 and 7.4.5.)	o	o	o	Section 10
Receive (Computer → PC CPU)	—	A PC CPU uses the FROM instruction to read data from the A1SJ71C24 buffer memory which was transmitted by a computer. When the A1SJ71C24 receives the data read completed signal from the sequence program, the A1SJ71C24 transmits a response message for the data receive to a computer.					

(b) Setting data length setting for data send

The length of the data to be transmitted between an A1SJ71C24 and a computer is set within the send message. (see Section 1.1.1 (2) (b)).

1) When data is transmitted to a computer:

When the data to be transmitted to a computer is output from the sequence program to an A1SJ71C24, the data length is written to the buffer memory of the A1SJ71C24.

The A1SJ71C24 sets the data length to a send message and transmits it along with the data to a computer.

This allows the length of a send message to vary according to the content and kind of data to be transmitted.

2) When data is received from a computer:

When an A1SJ71C24 receives data from a computer, the A1SJ71C24 writes the data length contained in the message to its buffer memory.

The sequence program reads the data length from the buffer memory to read all the received data.

POINT

The functions available with the bidirectional mode cannot be used together with the functions available with the no-protocol mode mentioned in Section 3.3.1 (2). Select either mode using the mode setting switch (see Section 4.3.1) and by setting the bidirectional mode setting area in the special applications buffer memory area (see Sections 3.5 and 10.2).

(4) Transmission error data read function

This function permits the sequence program to read error data when the error LEDs on the front panel of the module are lit and permits the sequence program to turn OFF an error LED which is lit. Section 7.3 gives details about sequence programs.

(a) Reading transmission error data

The display status of the error LEDs is stored in buffer memory. The sequence program can read this data to permit the PC CPU to execute error checking and interlocking with data communication sequence programs.

(b) Function to turn off error LEDs

This function permits the sequence program to turn off error LEDs which are lit without resetting the PC CPU.

3.3.2 Printer functions list

Table 3.5 Printer functions list

Function	Description	Reference
Printer message registration and reading functions by a computer	Fixed mesages of up to 80 characters can be registered and read out by using a CI (fixed message registration) command and a CJ (fixed message read) command in dedicated protocols 1 to 4 (modes 1 to 4).	Section 11.5
Printer message registration and reading functions by a sequence program	Fixed mesages or free messages of up to 80 characters can be registered and read out by using a sequence program.	Section 11.5
Printer output function	Fixed/free messages for designated data length can be output by a printer output request given from a sequence program.	Section 11.6
Printer test output function	Two kinds of test output is enabled by a printer output request given from a sequence program. (1) Registered fixed messages are output to the printer. (Registered message test output function) (2) ASCII codes (21H to 7EH) are output to the printer. (Printer test function)	Section 11.7 Section 11.8

3.4 I/O Signals List for CPU

The I/O signals of the A1SJ71C24 for the PC CPU are listed below. The numbers (n number) appended to X and Y are determined by the installing position of the A1SJ71C24 and the number of I/O signals used by the I/O signal signals used by the I/O modules installed in front of the A1SJ71C24. (Example: XnO → X0 when the A1SJ71C24 is loaded in slot 0 of the main base unit)

(1) Input signals (A1SJ71C24 → PC CPU)

There are 16 input signals: Xn0 to XnF are turned ON/OFF by the A1SJ71C24.

Table 3.6 Input Signals List

<table>
<tr><th rowspan="2">Input Signal</th><th rowspan="2">Signal Name</th><th colspan="3">Mode</th><th rowspan="2">Description</th><th rowspan="2">Reference Sections</th></tr>
<tr><th>Dedicated protocol</th><th>No-protocol/ Bidirectional</th><th>Printer function</th></tr>
<tr><td>Xn0</td><td>Send completed</td><td>—</td><td>○</td><td>—</td><td>Turns ON when the send from the A1SJ71C24 to the external device is completed when Y(n+1)0 is turned ON. Turns OFF when Y(n+1)0 is turned OFF.</td><td>9.2, 10.2</td></tr>
<tr><td>Xn1</td><td>Received data read request</td><td>—</td><td>○</td><td>—</td><td>Turns ON when the completed code, fixed length data, or designated data length is received from the external device. Turns OFF when Y(n+1)1 is turned ON.</td><td>9.2, 10.2</td></tr>
<tr><td>Xn2</td><td>Global signal</td><td>○</td><td>—</td><td>—</td><td>Turns ON/OFF according to the message (factor number) when a global command is received from a computer.</td><td>8.13</td></tr>
<tr><td>Xn3</td><td>On-demand function operating</td><td>○</td><td>—</td><td>—</td><td>Turns ON when the on-demand transmission is executed according to the request from the sequence program. Turns OFF when the on-demand transmission is completed.</td><td>8.14</td></tr>
<tr><td>Xn4 to Xn6</td><td>A1SJ71C24 message sequence state</td><td>○</td><td>—</td><td>—</td><td>(1) Indicates that a computer and an A1SJ71C24 are communicating with each other.
(2) Used by a sequence program to check communications status, etc.
<table>
<tr><th>Value</th><th>Xn6</th><th>Xn5</th><th>Xn4</th><th>Message Sequence State</th></tr>
<tr><td>0</td><td>OFF</td><td>OFF</td><td>OFF</td><td>A1SJ71C24 initializing after power ON or OFF using protocol 1 to 4</td></tr>
<tr><td>1</td><td>OFF</td><td>OFF</td><td>ON</td><td>Waiting for ENQ</td></tr>
<tr><td>2</td><td>OFF</td><td>ON</td><td>OFF</td><td>Received ENQ</td></tr>
<tr><td>3</td><td>OFF</td><td>ON</td><td>ON</td><td>Received station number (self)</td></tr>
<tr><td>4</td><td>ON</td><td>OFF</td><td>OFF</td><td>Waiting for response from PC after receiving all data</td></tr>
<tr><td>5</td><td>ON</td><td>OFF</td><td>ON</td><td>Waiting for message</td></tr>
<tr><td>6</td><td>ON</td><td>ON</td><td>OFF</td><td>Unused</td></tr>
<tr><td>7</td><td>ON</td><td>ON</td><td>ON</td><td>Unused</td></tr>
</table></td><td>—</td></tr>
</table>

Input Signal	Signal Name	Mode			Description	Reference Sections
		Dedicated protocol	No-protocol/ Bidirectional	Printer function		
Xn7	A1SJ71C24 READY signal	o	o	o	(1) Goes ON when the A1SJ71C24 is ready (after the power is turned ON, the PC CPU is reset, or the mode is changed). Turns ON when the A1SJ71C24 becomes READY after the PC CPU is reset after (a) power to the PC CPU was turned ON, or (b) the mode was switched. (Turns ON a few seconds after the power is turned ON.) Turns OFF when an error (which discontinues the A1SJ71C24's operation) occurs. (2) Used for the READY communications signal when the no-protocol mode, bidirectional mode, or the on-demand function of the dedicated protocol is used.	—
Xn8*	Printer processing completed	—	—	o	Turns ON when the message registration, read, or output to the printer is completed after Y(n+1)8 is turned ON. Turns OFF when Y(n+1)8 is turned OFF.	11
Xn9	Mode change completed	o	o	o	Goes ON when completing the A1SJ71C24 mode change turns ON the X(n+1)9.	6
XnA to XnC	—	—	—	—	Unavailable	—
XnD	Watch dog timer error	o	o	o	Turns ON when the A1SJ71C24 watch dog timer error occurs. Remains OFF during normal operation.	11.2
XnE · XnF	—	—	—	—	Unavailable	—

* Xn8 is available only for A1SJ71C24-PRF (with printer function). It is unavailable for A1SJ71C24-R2.

(2) Output signals (PC CPU → A1SJ71C24)

There are 16 output signals: Y(n+1)0 to Y(n+1)F are turned ON/OFF by the A1SJ71C24.

Table 3.7 Output Signals List

Output Signal	Signal Name	Mode			Description	Reference Sections
		Dedicated protocol	No-protocol/ Bidirectional	Printer function		
Y (n+1) 0	Send request	–	o	–	When this signal is turned ON by the sequence program in the no-protocol mode/bidirectional mode, data written to the buffer memory is transmitted from the A1SJ71C24 to an external device. (After Xn0 is turned ON, Y(n+1)0 is turned OFF.	9.2, 10.2
Y (n+1) 1	Received data read completed	–	o	–	This signal turns ON in the no-protocol mode/bidirectional mode, when the PC CPU has completed reading the data received from an external device. This data is stored in the A1SJ71C24 buffer memory. (After Xn1 is turned OFF, Y(n+1)1 is turned OFF.	9.2, 10.2
Y (n+1) 2 to Y (n+1)7	–	–	–	–	Unusable	–
Y (n+1) 8*	Printer processing request	–	–	o	Starts massage registration, read, or output to the printer by turning ON this signal.	11
Y(n+1) 9	Mode change request	o	o	o	Turning this ON (using the sequence program) changes the A1SJ71C24 mode, which executes the initial processing. Goes OFF after turning ON Xn9.	6
Y(n+1)A · Y(n+1) B	–	–	–	–	Unusable	–
Y (n+1) C*	Printer processing interrupt	–	–	o	Interrupts output to the printer by truning ON this signal. Restarts output to the printer by turning OFF this signal.	11
Y (n+1) D · Y (n+1) F	–	–	–	–	Unusable	–

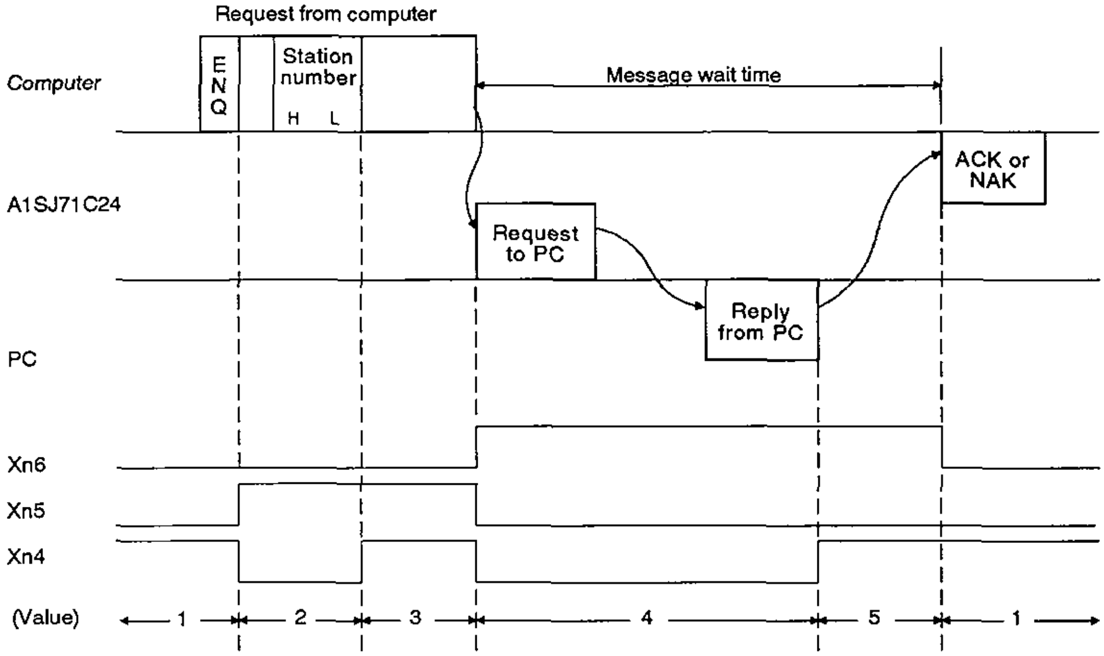
* Y (n+1) 8 and Y (n+1) C are available only for A1SJ71C24-PRF (with printer function).
They are unavailable for A1SJ71C24-R2.

IMPORTANT

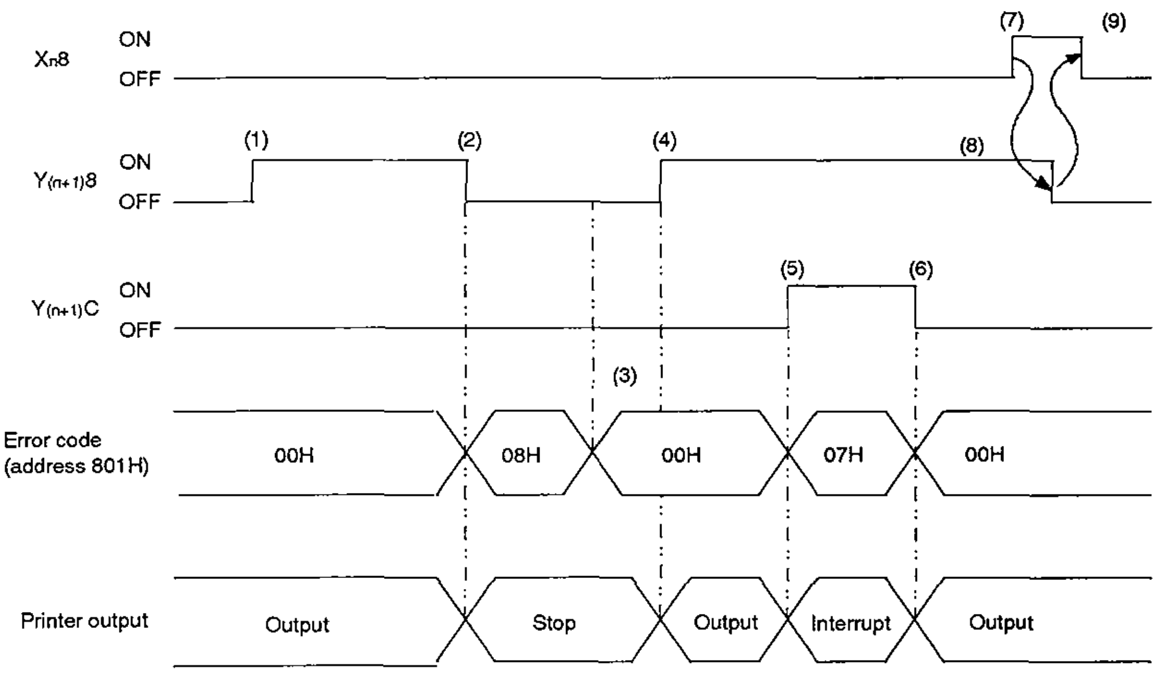
Y(n+1)2 to Y(n+1)7 Y(n+1)A, Y(n+1)B and Y(n+1) D to Y(n+1)F are reserved for system use only. A1SJ71C24 functions cannot be guaranteed if these signals are turned ON or OFF by a sequence program.

REMARKS

Example 1: Use of input signals Xn4 to Xn6.



Example 2: *Use of Xn8, Y(n+1)8, and Y(n+1)C when printer function is used.*



- Operation contents

(1) When $Y_{(n+1)}8$ is turned ON, the message output to the printer is started.

(2) When $Y_{(n+1)}8$ is turned OFF, the message output to the printer is forcibly completed. At this time, an error(08H) occurs.

(3) 00H is written to buffer address 801H and an error is reset.

(4) When $Y_{(n+1)}8$ is turned ON, the message output to the printer is started.

(5) When $Y_{(n+1)}C$ is turned ON, the message output to the printer is interrupted. At this time, an error(07H) occurs.

(6) When $Y_{(n+1)}$ is turned OFF, the interrupted messages are output to the printer. At this time, an error is automatically reset to 00H.

(7) When the message output is completed, X_n8 is turned ON.

(8) $Y_{(n+1)}8$ *is turned OFF by a sequence program.*

(9) When $Y_{(n+1)}$ 8 is turned OFF, $X_{(n+1)}8$ is turned OFF.

3.5 Buffer Memory Applications and Allocation

The term "buffer memory" used in this manual refers to a memory area of an A1SJ71C24 used to store the control and communications data which is transmitted between an external device (e.g., a computer) and a PC CPU.

The buffer memory can be accessed from the sequence program by using the FROM/TO instruction.

The buffer memory can be accessed from an external device by using the buffer memory read/write command (CR, CW) with dedicated protocols 1 to 4.

(1) Buffer memory applications

There are two types of buffer memory area. One area may be used freely by the user, but the other area has a special application.

(a) User area

There are four applications of the user area, which can be categorized as follows.

1) Data receive area in no-protocol mode/bidirectional mode

This area stores data transmitted from an external device in the no-protocol mode or bidirectional mode.

2) No-protocol mode/bidirectional mode data send area

This area stores data from the PC CPU to be transmitted to an external device.

3) On-demand data storage area

This area stores send data to be transmitted from the sequence program to an external device using the on-demand function.

4) Area when using buffer memory read/write commands

This area stores data when communication is made using protocols 1 to 4 for buffer memory read/write commands (CR,CW).

(b) Special applications area

The applications of this memory area are fixed. They are used to determine the data communications format and to change the allocation of the memory area for section (a) above.

When the power is turned ON or the PC CPU is reset, default values are written to this special applications area.

Default values can be changed to suit the purposes and applications of data transmission and the specifications of the external device. Section 7 gives details.

(2) Buffer memory allocation

The buffer memory consists of 16-bit addresses. The buffer memory has no back-up battery.

The buffer memory address names and values for each address are listed in the following table.

IMPORTANT

Buffer memory addresses 10EH, 11DH to 11FH are reserved for system use only. Data written to this area will prevent correct operation of the A1SJ71C24.

The following table shows the contents of the buffer memory allocation.

The memory areas which are used with the no-protocol mode or the bidirectional mode are listed as those to be used with the no-protocol mode.

The memory areas function the same way in either mode. When the bidirectional mode is required, see the following table, changing "no-protocol" to "bidirectional".

Table 3.8 Buffer Memory

Addresses	Buffer Memory Address Names		Default Values	Mode set by user: Dedicated Protocol	No-Protocol	Bidirectional	Printer	(Reference Sections)
0H	User area (256 words) / Area for default: No-protocol send data length storage area	No-protocol send area	0	o *3	o	o	o	
1H to 7FH	No-protocol send buffer memory area (Send data storage area)	No-protocol send area			o	o	o	
80H	No-protocol received data length storage area.	No-protocol receive area			Δ	Δ	Δ	
81H to FFH	No-protocol receive buffer memory area (Received data storage area)	No-protocol receive area			Δ	Δ	Δ	
100H•	Area to specify receive completed code in no-protocol mode		0D0AH (CR, LF)	—	o	—	—	7.4.1
101H	Error LED display OFF state storage area		0	Δ	Δ	Δ	Δ	7.3.1
102H	Error LED turn OFF request area		0	o	o	o	o	7.3.2
103H•	Area to specify word or byte units in no-protocol mode		0 (words)	o *1	o	o	—	7.4.3
104H•	Area to specify head address of send buffer memory for no-protocol mode		0	—	o	o	—	7.4.4
105H•	Area to specify send buffer size for no-protocol mode		80H	—	o	o	—	
106H•	Area to specify head address of receive buffer memory for no-protocol mode		80H	—	o	o	—	7.4.5
107H•	Area to specify receive buffer size for no-protocol mode		80H	—	o	o	—	
108H•	Area to specify receive completion 1 on data length in no-protocol mode		127 (words)	—	o	—	—	7.4.2
109H	Area to specify head address of on-demand buffer memory		0	o	—	—	—	8.14
10AH	Area to specify on-demand buffer size		0	o	—	—	—	
10BH•	Area to specify RS-232C CD terminal check		0 (check CD terminal)	o	o	o	—	7.1
10CH	Storage area for on-demand errors		0	Δ	—	—	—	8.14
10DH	Receive data clear request area for no-protocol mode		0	—	o	—	—	9.5
10EH	System area (unavailable)		—	—	—	—	—	—
10FH•	RS-232C communications mode setting area		0 (Full-duplex transmission)	o	o	o	—	7.2
110H•	Simultaneous send priority/non-priority setting area*2		0 (Priority)	o	o	o	—	
111H•	Send method setting area when transmission is resumed*2		0 (No retransmission)	o	o	o	—	
112H•	Bidirectional mode setting area		0 (No-protocol mode)	—	—	o	—	7.5
113H•	Time-out check time setting area		0 (Infinite)	—	—	o	—	
114H•	Simultaneous transmission data valid/invalid setting area		0 (Data valid)	—	—	o	—	
115H•	Check sum enable/disable setting area		0 (Check sum enabled)	—	—	o	—	
116H	Data send error storage area		0	—	—	Δ	—	10.2
117H	Data receive error storage area		0	—	—	Δ	—	

Addresses	Buffer Memory Address Names	Default Values	Mode set by user: Dedicated Protocol	No-Protocol	Bidirectional	Printer	(Reference Sections)
118H	Mode setting state storage area	0 (Mode 0) *5	Δ	Δ	Δ	—	7.6
119H	Mode change specification area	0 (No change) *6	o	o	o	—	
11AH•	Transmission control specification area (DC/DTR control)	0 (DTR control)	—	o	o	o	7.7
11BH•	DC1/DC3 control code specification area	1311H	—	o	o	o	
11CH•	DC2/DC4 control code specification area	1412H	—	o	o	o	
11DH to 11FH	System area (Unusable)	—	—	—	—	—	—
120H to DFFH	*7	0	o *3	o *3	o *3	o *3	

*4

*1: The unit of the transmission (send/receive) data in the no-protocol mode or bidirectional mode or of the send data when the on-demand function of the dedicated protocol is used.

*2: Set this when the RS-232C interface is set to half-duplex communications.

*3: Areas should be allocated so that they do not overlap with each other when (a) data is transmitted in the no-protocol mode or bidirectional mode, or (b) when more than one function of data transmission using the on-demand function of the dedicated protocol is used.

*4: Change the default values marked by the dot symbol (•) attached to the right of the address only when the READY signal of the A1SJ71C24 is turned ON after the power is turned ON or the PC CPU is reset.

Or, change the values when the higher bytes of the mode switching designation area of the buffer are changed after the A1SJ71C24 READY signal is turned ON by switching the mode of A1SJ71C24.

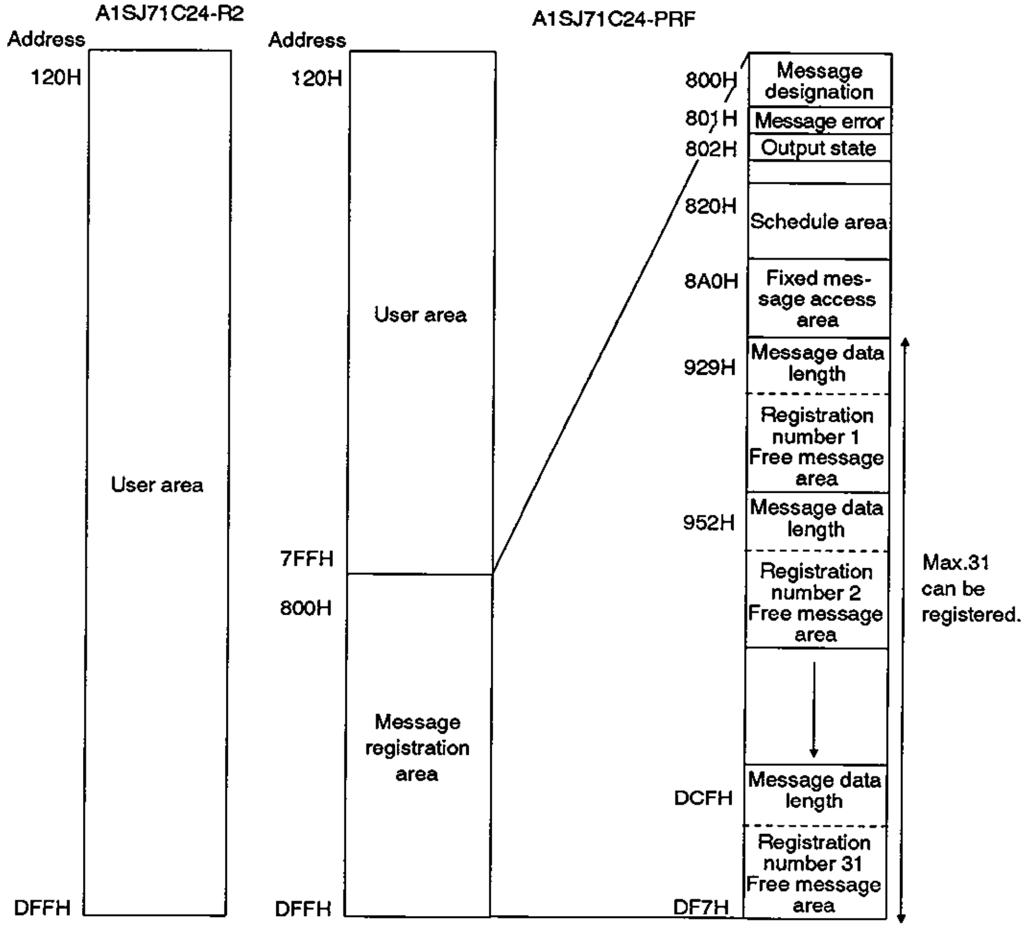
*5: The value (1H to DH) corresponding to the set value (1 to D) of mode setting switch (see Section 4.3) is stored as default value.

*6: 0 is stored before switching the mode.

The value (1H to DH) of mode number corresponding the present mode is stored after switching the mode.

1H to DH correspond to the set value (1 to D) of mode setting switch (see Section 4.3).

*7: 120H to DFFH are allocated to the user area in an A1SJ71C24-R2.
120H to 7FFH are allocated to the user area and 800H to DFFH are allocated to the message registration area in an A1SJ71C24-PRF as shown below.



4. SETTINGS AND PROCEDURES BEFORE OPERATION

4.1 Settings and Procedures before Operation

The settings and procedures which have to be done before a system using the A1SJ71C24 can be started are described below.

Determine the system configuration ......See Section 2.3.

↓

Set up the hardware

(1) Set the transmission specifications ......See Section 4.3.2.
- Specify the data length
- Specify the transmission speed
- Specify the parity check
- Specify odd or even parity
- Specify the number of stop bits
- Specify the sum check
- Specify write during RUN

(2) Set the transmission control protocol ......See Section 4.3.1.

↓

Self loopback test ......See Section 4.6.

↓

External wiring ......See Sections 3.2, 4.5.

↓

Loopback test ......See Sections 4.3, 8.15.

↓

Ilnitialize using a sequence program ......See Section 7.

↓

Create a data communications program ..... A sequence program for data transmission is required to use the following functions:
- Data transmission in the no-protocol/ bidirectional mode
- Data transmission using the on-demand function of the dedicated protocol
- Signal input using the global function of the dedicated protocol

↓

Operation

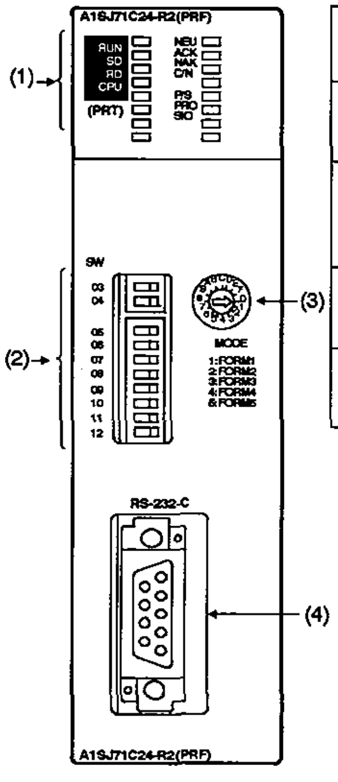
REMARKS

(1) Appendix 10 contains the form sheet for recording the setting values of the A1SJ71C24.

(2) Section 11.1 gives the procedure for using the printer function.

4.2 Nomenclature

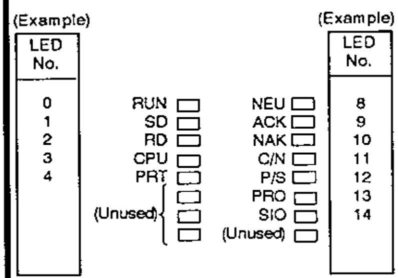
4.2.1 Nomenclature



No.	Name	Description	Reference Sections
(1)	Indicator LEDs	Display the operating status, computer communications underway, and alarms.	4.2.2
(2)	Transmission specification setting switches	Used to set data bit, parity presence absence, stop bit, sum check, etc.	4.3.2
(3)	Mode setting switch	Switch for selecting transmission control protocol	4.3.1
(4)	RS-232C connector	RS-232C connector for linking A1SJ71C24 with computer.	3.2.2 4.5.2

4.2.2 LED signals and displays

LED Area Details



LED No.	LED	Meaning of LED Display	LED ON	LED OFF	Initial Status of LED
0	RUN	Normal run	Normal	Error	ON
1	SD	Transmitting	Flashes during data transmission		OFF
2	RD	Receiving	Flashes during data receive		OFF
3	CPU	Communications with PC CPU	Flashes during communications with PC CPU		ON
4	PRT *1	Printer message output	Turns ON when printer messages are output		OFF
8	NEU	Neutral	Transmission sequence initial state (waiting for ENQ)	ENQ received	*2
9	ACK	ACK	After sending ACK	After sending NAK	OFF
10	NAK	NAK	After sending NAK	After sending ACK	OFF
11	C/N	Result of PC CPU communications		Normal	OFF
12	P/S	Parity/sum check errpr	Parity/sum check error	Normal	OFF
13	PRO	Protocol error	Communications protocol error	Normal	OFF
14	SIO	SIO error	Overrun, framing error	Normal	OFF

*1 is applied to A1SJ71C24-PRF.
*2 varies according to the switch setting as shown in the following table.

LED No.	Name \ Mode Setting	1 to 4	5	F
8	NEU	ON	OFF	OFF

(1) LEDs C/N to SIO (LED Nos.11 to 14) above light when an error occurs.

The ON/OFF status of the LED Nos. 11 to 14 are stored in the buffer memory at address 101H. The status can be read using the PC CPU instruction which permits checking by a sequence program.

(2) After any LED C/N to SIO (LED Nos. 11 to 14) is ON, they remain ON even when the cause of the error is eliminated.

It is necessary to send a turn-off request to address 102H of the buffer memory using the sequence program TO instruction to turn OFF the LED.

(3) LEDs RUN to NAK (LED Nos. 0 to 10) above light corresponding to the relevant status.

(4) LEDs C/N (LED Nos. 11) above light in the following circumstances:

(a) When the A1SJ71C24 attempts to make an illegal access while the PC CPU is running (a write during program execution, for example).

(b) During abnormal PC CPU access.

(5) The "initial state" column indicates the status when the power is turned ON the PC CPU is reset or when the READY signal of the A1SJ71C24 is turned ON after the mode was switched.

4.3 Settings

This section describes the setting methods and explains the settings of the transmission control protocol and communications specifications (data length, sum check, etc.).

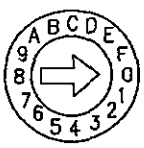
After changing the settings, turn the PC CPU power supply OFF and back ON, or reset the PC CPU.

4.3.1 Setting the dedicated protocol, no-protocol mode, bidirectional mode or printer function

(1) The method of setting the transmission control protocol and the meaning of the switch settings are described in the table below.

When the mode switch is set to "5" and the bidirectional mode setting area in the buffer memory is set to "1", the no-protocol mode in the following table changes to the bidirectional mode.

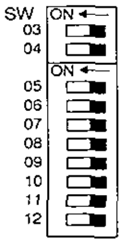
All mode settings in the following table are in the no-protocol mode.

Mode Setting Switch	Mode Setting Switch Number	Mode Settings	Notes
	0	Unusable	
	1	Protocol 1	For connection of computers to RS-232C.
	2	Protocol 2	
	3	Protocol 3	
	4	Protocol 4	
 MODE	5	No-protocol or Printer function	This mode is used to enable a no-protocol computer link with all devices connected to the RS-232C interfaces. Or, this mode is used to the printer function with the A1SJ71C24-PRF.
	6 to E	Unusable	
	F	For module test	This mode is used for testing the module.

POINT

Sections 2.3.1 to 2.3.2 give the examples of settings with different system configurations.

4.3.2 Setting of transmission specifications

Setting of Switches	Switches	Setting Items	Position of Setting Switch								Remarks
			ON				OFF				
	SW03	Unused	—				—				—
	SW04	Write during RUN enabled/disabled setting	Enabled				Disabled				—
		Transmission speed setting — Baud rate	300	600	1200	2400	4800	9600	19200	Un-usable	—
	SW05		OFF	ON	OFF	ON	OFF	ON	OFF	ON	
	SW06		OFF	OFF	ON	ON	OFF	OFF	ON	ON	
	SW07		OFF	OFF	OFF	OFF	ON	ON	ON	ON	
	SW08	Data bit setting	8 bits				7 bits				—
	SW09	Parity bit setting	Set				Not set				—
	SW10	Even/odd parity setting	Even				Odd				Valid when parity bit is set.
	SW11	Stop bit setting	2 bits				1 bit				—
	SW12	Sum check setting	Set				Not set				—

(1) Write during RUN

Set whether a processing requested by the external device is executed or not executed by the PC CPU in the RUN state when the computer link operates with the dedicated protocol.

Section 3.3.1 gives the functions available with this setting.

(2) Transmission specifications

Do not set the "unusable" baud rate setting (SW13, 14, and 15 ON).

If these switches are set, the RUN indicator LED (LED No. 0) is turned OFF and operation is not possible.

(3) Sum check

Set whether the sum check code is added or not added to the end of the message, when the computer link operates with the dedicated protocol.

Sections 8.4.1 to 8.4.4 and 8.4.5 (7) give the message structure and sum check code when the sum check setting is "Enabled".

4.4 Loading and Installation

4.4.1 Handling instructions

(1) Protect the A1SJ71C24 and its terminal block against impact.

(2) Do not touch or remove the printed circuit board from the case.

(3) Do not allow metal particles or wire offcuts to enter the A1SJ71C24.

(4) Tighten the module mounting and terminal screws as specified below.

Screw	Tightening Torque kg·cm(lb·inch)
Module mounting screws (M4)	78 to 117 N·cm {8(6.93) to 12(10.39)}

4.4.2 Installation environment

Never install the system in the following environments:

(1) Locations where ambient temperature is outside the range 0 to 55°C (32 to 131°F).

(2) Locations where ambient humidity is outside the range of 10 to 90%RH.

(3) Locations where dew condensation takes place due to sudden temperature changes.

(4) Locations where there are corrosive gasses and combustible gasses.

(5) Locations where there is a high level of conductive powder, such as dust and iron filings, oil mist, salt, and organic solvent.

(6) Locations exposed to the direct rays of the sun.

(7) Locations where strong power and magnetic fields are generated.

(8) Locations where vibration and shock are directly transmitted to the main unit.

4.5 External Wiring

4.5.1 Precautions during wiring

External wiring which is resistant to external noise effects is a prerequisite for reliable A1SJ71C24 operations (full use of all available functions).

When doing external wiring of the A1SJ71C24, the following precautions must be taken:

(1) Keep main circuit wiring, high-voltage wiring, and other load-carrying wiring outside the PC CPU separate from A1SJ71C24 wiring. Never bundle them together. This prevents noise and surge-induction effects.

(2) Ground the shield of shielded wires and cables at only one point.

4.5.2 Connecting the RS-232C connectors

Precautions and examples of connections to an RS-232C connector is shown in the diagram below.

(1) Precautions during connections

If half-duplex transmission (see Section 7.2 for the setting method) is used, perform wiring so that the CD signal of the A1SJ71C24 can be controlled by the external device.

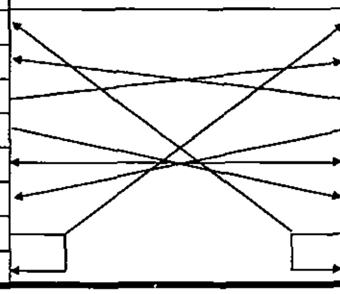
Also, set the A1SJ71C24 to execute the CD terminal check (see Section 7.1).

Section 5.4 gives the ON/OFF timing control of the CD signal of the A1SJ71C24 using the external device.

(2) Examples

(a) Connections to a device which can turn the CD terminal signal ON (for full-/half-duplex transmissions)

A1SJ71C24		Cable Connections and Signal Directions	External Device
Signal Names	Pin Numbers		Signal Names
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)

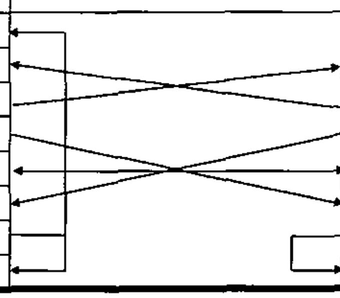


(b) Connections to a device which cannot turn the CD terminal signal ON (for full-duplex transmission)

1) When wired as in step (a) above, disable the RS-232C CD terminal check.

2) If the RS-232C CD terminal check function is enabled, wire the connectors as shown below.

A1SJ71C24		Cable Connections and Signal Directions	External Device
Signal Names	Pin Numbers		Signal Names
CD	1		CD
RD(RXD)	2		RD(RXD)
SD(TXD)	3		SD(TXD)
DTR(ER)	4		DTR(ER)
SG	5		SG
DSR(DR)	6		DSR(DR)
RS(RTS)	7		RS(RTS)
CS(CTS)	8		CS(CTS)



POINT

When connecting to the printer, use the connections to a device which cannot turn the CD terminal signal ON (described in (b) above).

4.6 Self-loopback Test

The self-loopback test function is used (when the A1SJ71C24 is not connected to the computer) to check that the A1SJ71C24 module is operating normally. This function is selected by setting the mode setting switch to "F".

4.6.1 Procedure to carry out the self-loopback test

The procedure to carry out the self-loopback test is as follows:

Step 1 Connect the cables

Connect cables to the RS-232C connectors as shown below.

A1SJ71C24		Cable Connections
Signal Names	Pin Number	
CD	1	
RD	2	
SD	3	
DTR	4	
SG	5	
DSR	6	
RS	7	
CS	8	

Step 2 Set the mode setting switch

Set the mode setting switch to "F" to select the self-loopback test. (Section 4.3.1 tells details of how to set this switch.)

Step 3 Execute the self-loopback test

(1) Turn the PC CPU power supply ON or reset the PC CPU.

The test starts automatically when the A1SJ71C24 READY signal turns ON. The READY signal turns ON a few seconds after the power supply is turned ON or the PC CPU is reset.

(2) Check sequence

Checks are executed out in the following order:

1) PC CPU communications check

2) RS-232C communications check

The checks are then repeated. The checks are completed within one second. The checks are executed automatically by the A1SJ71C24.

(3) Check the LED display status, as described in Section 4.6.2.

Normal : Follow procedure (4) to end the test.

Error : Correct the error and repeat the self-loopback test

(4) When checks are completed:

1) Turn the power supply OFF.

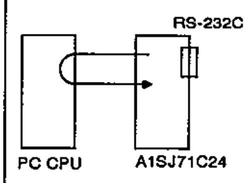
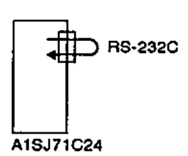
2) Disconnect the cables. Connect the cables to link with the computers.

3) Change the setting of the mode setting switch. ("1" to "5")

POINT

Two A1SJ71C24 modules can be loaded to A1SCPU. However, do not execute the self-loopback test with both modules simultaneously (this will result in a PC CPU communications check error).

4.6.2 Self-loopback test operations

Check Items	Check Descriptions	Normal Indicator LED		Error Indicator LED		Information Flow
PC CPU communication check	After writing data to special data register D9072, the A1SJ71C24 reads and verifies it. If the data matches, it is changed and the procedure is repeated. If data does not match, an error is indicated.	C/N (LED No. 11)	OFF	C/N (LED No. 11)	ON	
		CPU (LED No. 3)	Flashing			
RS-232C communications check	Checks data sent from RS-232C connector. If normal, A1SJ71C24 changes data and the procedure is repeated. If not normal, an error is indicated. An error is indicated if no cable is connected.	SIO (LED No. 14)	OFF	SIO (LED No. 14)	ON	
		SD (LED No. 1)	Flashing			
		RD (LED No. 2)				

*The test continues even if an error occured with a checking item.

4.7 Loopback Test

The loopback test checks the correctness of data communications between the computer and the A1SJ71C24 using the dedicated command (TT) with the dedicated protocols 1 to 4.

The procedure to execute the loopback test is as follows:

Step 1 Connect the computer and A1SJ71C24

Connect the cable between the computer and A1SJ71C24 as described in Section 4.5.

Step 2 Mode switch settings

Set the mode switch to "1" to "4" to set the testing interface for the dedicated protocol. (Section 4.3.1 gives detail of the setting method.)

Step 3 PC CPU start-up

Turn the power to the PC CPU ON or reset the PC CPU. The A1SJ71C24 ready signal turns ON (ready for operation), after which the loopback test can be executed.

(The ready signal turns ON at a few seconds after the A1SJ71C24 is turned ON or reset.)

Step 4 Execute the loopback test command

(1) Create a program to be tested and transmit the command and data to the A1SJ71C24.

Section 8.4 gives the message structure of formats 1 to 4, and Section 8.15 gives the loopback command (TT).

(2) The A1SJ71C24 transmits the unchanged data back to the computer.

Step 5 Computer consistency check

(1) Check at the computer if data transmitted from the computer to the A1SJ71C24 is identical with the data transmitted back from the A1SJ71C24 to the computer.

Identical data indicates that the communication between the computer and A1SJ71C24 is normal.

If the data transmitted from the computer to the A1SJ71C24 and the data transmitted back from the A1SJ71C24 to the computer are not identical, the transmission specification settings probably do not match or the CD terminal is repeatedly turning ON/OFF. Use the troubleshooting charts in Sections 11.2.5 and 11.2.6 to determine and correct the problem. Then repeat the loopback test.

(2) If data communications is not possible

The hardware settings or cable connections have probably not been done correctly.

Use the troubleshooting charts in Sections 11.2.2, 11.2.3, and 11.2.4 to determine and correct the problem and then repeat the loopback test.

(3) After the loopback test is finished, a computer link which uses the dedicated protocol is enabled.

When a computer link uses the no-protocol/bidirectional mode, do the following:

- Set the mode switches.
- Turn the power to the PC CPU OFF/ON or reset the PC CPU.

After doing the above, the computer link operation is enabled.

4.8 Inspection and Maintenance

The A1SJ71C24 module itself requires no particular inspection procedures. However, carry out the inspections listed in the PC CPU User's Manual to ensure optimum system performance.

[COMPUTER LINK FUNCTIONS]

This section describes the communications procedures, link method, and commands used with the computer link of the A1SJ71C24-R2 and A1SJ71C24-PRF.

5. HALF-DUPLEX COMMUNICATIONS USING THE RS-232C INTERFACE

This section explains how to do half-duplex communications using an RS-232C interface to connect an external device and an A1SJ71C24.

This section does not apply to full-duplex communications.

A1SJ71C24 can do half-duplex communications with an external device by using the RS-232C interface by setting buffer memory.

While receiving data from an external device in half-duplex communications, data is not transmitted from the A1SJ71C24 to the external device.

The key points for doing half-duplex communications between an external device and the A1SJ71C24 using the RS-232C connector are as follows:

- System configurations and functions
- Buffer memory settings
- Wiring
- ON/OFF timing of the CD and RS signals of the A1SJ71C24

5.1 System Configurations and Functions

The following figure shows (a) the system configurations of the external device and the PC CPU that can do half-duplex communications, and (b) the functions of the A1SJ71C24

Functions / System Configurations (external device : PC CPU)	Dedicated Protocol		No-protocol Mode/bidirectional Mode
	Data Communications by a Command Transmitted from the External Device	Data Send from the PC CPU by the On-demand Function	Data Send and Data Receive
1 : 1	o	o*1	o*2

o: Usable
x: Unusable

*1 During data communicates, the send timing of data that a sequence program requested to send changes due to the on-demand function.

See Section 8.14.2.

The send timing also changes as mentioned in *2 below.

*2 Send timing of data sent from the A1SJ71C24 and the external device changes according to the set timing of "priority/non-priority at the simultaneous transmission" set with the A1SJ71C24.

See Section 5.4.

5.2 Buffer Memory Settings

The following describes the buffer settings of the A1SJ71C24 for doing half-duplex communications.

Perform the following settings with the sequence program only when the A1SJ71C24 READY signal is turned ON after the A1SCPU is reset or when the A1SCPU is turned ON.

Section 7.2 gives setting details.

(1) Communications setting using the RS-232C interface (Address 10FH)

Set "1" to do half-duplex communications.

(2) Setting of priority/non-priority at the simultaneous transmission (Address 110H)

When the A1SJ71C24 and the external device begin transmitting data simultaneously in half-duplex communications, designate (a) continuation (priority) of the send from the A1SJ71C24, or (b) interruption (non-priority).

Set "0" to designate " priority ".

Set "1" to "255" to designate " non-priority ".

This set value is the send wait time (unit :10 msec), until data transmission starts, after the data send state is restarted.

POINT

When an A1SJ71C24 is set to " priority ", the A1SJ71C24 keeps on transmitting data and ignoring received data. Even if data is transmitted from the external device after the A1SJ71C24 has started data transmission.

The external device that transmits data must execute the following so that the A1SJ71C24 does not ignore received data:

- Transmit response messages to start communications
- Resend data when a time out error of a response message occurs.

(3) Setting the method of resend (Address 111H)

When setting " half-duplex communications "+" non-priority " according to (1) and (2), this setting becomes valid.

As for simultaneous transmission from the external device and the A1SJ71C24, when the A1SJ71C24 restarts the send after interruption of the send, designate whether the interrupted message is transmitted again from the beginning ("resend") or only the remaining part is transmitted ("not resend").

Set "1" to designate " resend ".

Set "0" to designate " not resend ".

5.3 Wiring

The following describes the wiring for connecting the external device to the A1SJ71C24.

To do half-duplex communications, the CD signal of the A1SJ71C24 must be controlled by the external device.

Connect them according to "Connections to a device which can turn the CD terminal signal ON" shown in Section 4.5.2.

Section 5.4 describes the ON/OFF timing of the CD signal of the A1SJ71C24.

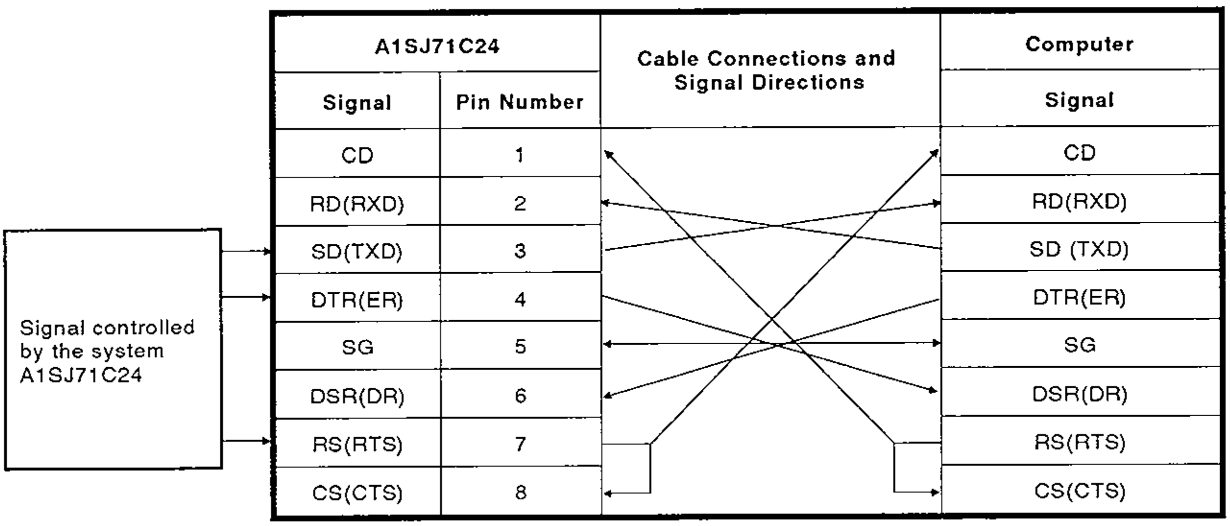
5.4 ON/OFF Timing of the CD and RS Signals of the A1SJ71C24

When doing half-duplex communications, the data transmission timing is shown by using the CD and RS signals of the A1SJ71C24.

In half-duplex communications, an external device controls the CD signal of the A1SJ71C24.

The A1SJ71C24 system controls the RS signal of the A1SJ71C24.

The table below shows the half-duplex communications connections discussed in this section.



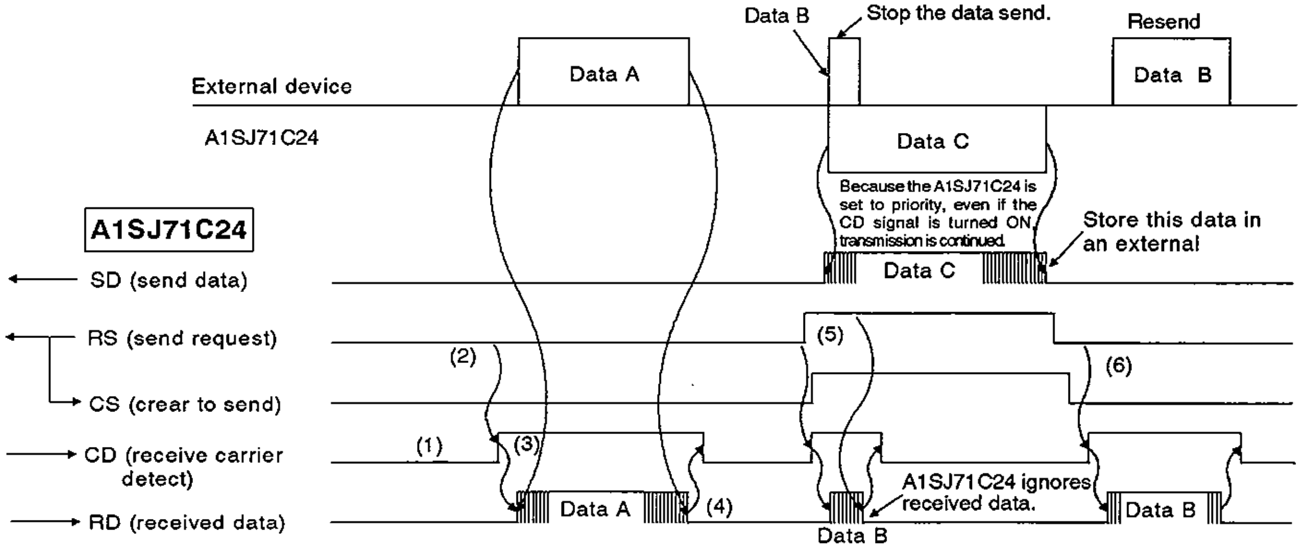
Example of Connections

5.4.1 Data transmission timing from an external device

When doing half-duplex communications, the data transmission timing from the external device is shown by using the CD and RS signals of the A1SJ71C24.

Setting the buffer memory of the A1SJ71C24 to "priority/non-priority at simultaneous transmission" controls the CD signal of the A1SJ71C24.

(1) A1SJ71C24 is set to " priority ".



The following steps describe the operations required for an external device at every timing mentioned by 1) to 6) in the above figure.

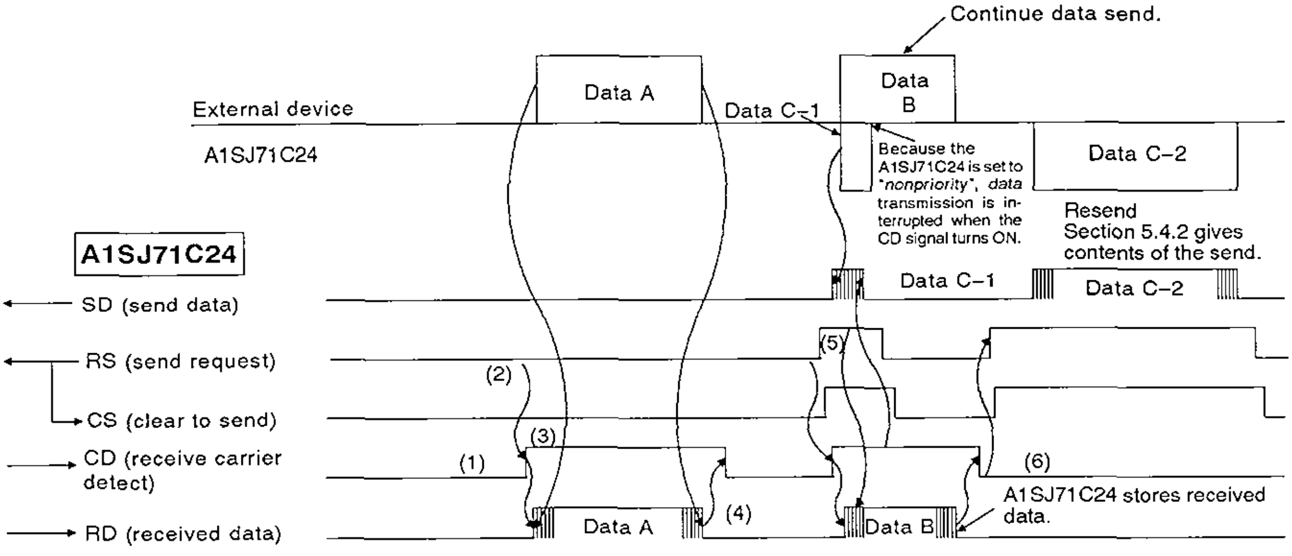
The signal names are of the signals of the A1SJ71C24.

1) When not transmitting data from the external device to the A1SJ71C24, turn the CD signal OFF.
2) When doing a data send, check the RS signal. If the RS signal is OFF, turn the CD signal ON.
   If the RS signal is ON, wait until it turns OFF. After the RS is turned OFF, turn the CD signal ON.
3) After turning the CD signal ON, transmit data.
4) After completing the data send, turn OFF the CD signal .
5) If the RS signal turns ON during the data send, stop the data send. Then, turn the CD signal OFF, and perform data receive processing. (When the A1SJ71C24 and an external device start data transmission simultaneously, the RS signal turns ON.)
6) Retransmit all interrupted data from the external device to the A1SJ71C24 after the data send from the A1SJ71C24 is completed.

REMARK

When (a) starting or during data transmission to the A1SJ71C24, (b) if the DTR(ER) signal of A1SJ71C24 turns OFF or when a DC3 code is received, interrupt data transmission until the DTR signal turns ON or until a DC1 code is received.
See Appendix 4.

(2) *A1SJ71C24 is set to "non-priority".*



The following steps describe the operations required for an external device at every timing mentioned by 1) to 6) in the above figure.

The signal name is the signal of the A1SJ71C24.

As described in (1), turn ON/OFF the CD signal of the A1SJ71C24 with the external device and do data transmission to the A1SJ71C24.
(Note that 5) and 6) are different in the non-priority setting.)

1) When not transmitting data from the external device to the A1SJ71C24, turn the CD signal OFF.
2) When doing a data send, check the RS signal. If the RS signal is OFF, turn the CD signal ON.
   If the RS signal is ON, wait until it turns OFF. After the RS is turned OFF, turn the CD signal ON.
3) After turning the CD signal ON, transmit data.
4) After completing the data send, turn OFF the CD signal.
5) Even if the RS signal turns ON during data transmission, continue the data send to the A1SJ71C24. (This occurs when the A1SJ71C24 and the external device start data transmission simultaneously.)
6) After the send from the external device is completed, transmit data from the A1SJ71C24 to the external device.
   Section 5.4.2 gives details.

REMARK

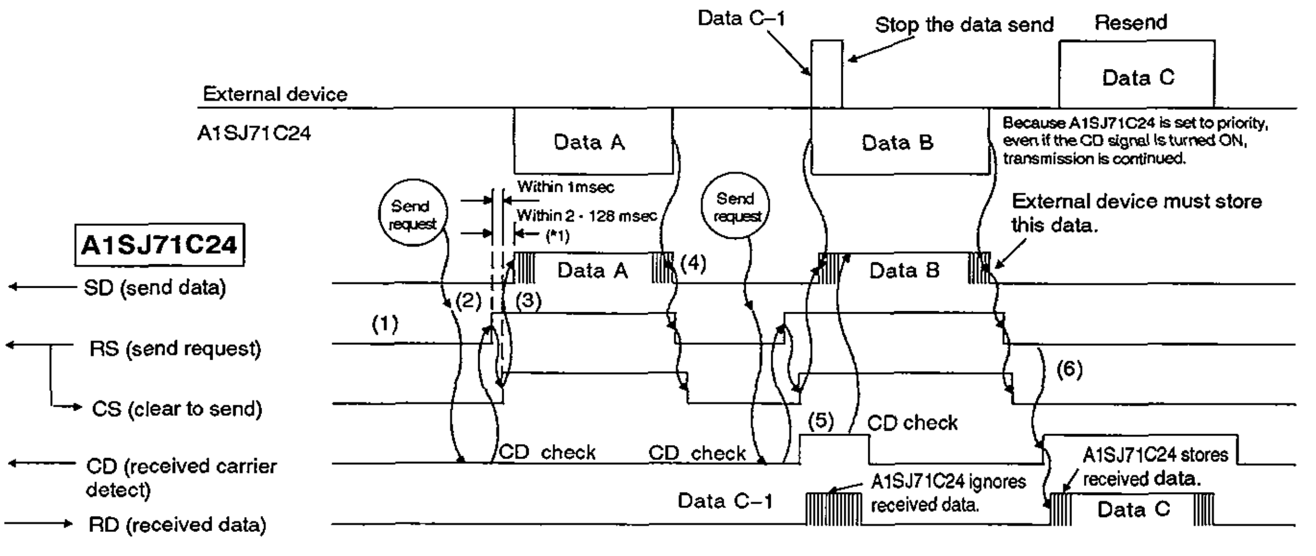
When (a) starting or during data transmission to the A1SJ71C24, and (b) if the DTR(ER) signal of A1SJ71C24 turns OFF or when a DC3 code is received, interrupt data transmission until the DTR signal turns ON or until a DC1 code is received.
See Appendix 4.

5.4.2 Data transmission timing from an A1SJ71C24

When doing half-duplex communications, data transmission timing from an A1SJ71C24 is shown by using the CD signal and RS signal of the A1SJ71C24.

Control the CD signal of the A1SJ71C24 by setting the buffer memory of the A1SJ71C24 to "priority/non-priority at simultaneous transmission" for data transmission.

(1) A1SJ71C24 is set to " priority ".



The following steps describe the operation at every timing mentioned by (1) to (6) in the above figure.

The signal names are of the signals of the A1SJ71C24.

As described in (1), turn ON/OFF the RS signal of the A1SJ71C24 with the external device and transmit data to the A1SJ71C24.

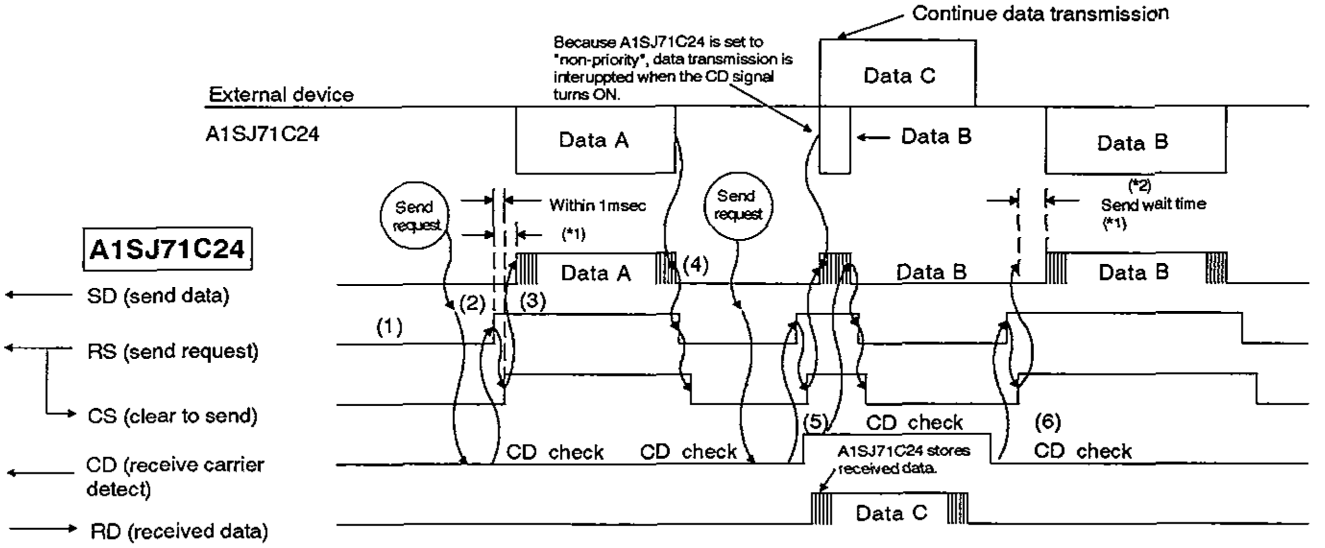
1) When not transmitting data from the external device to the A1SJ71C24, turn the RS signal OFF.
2) When doing a data send, check the CD signal. If the CD signal is OFF, turn the CD signal ON.
   When the CD signal is ON, wait until it turns OFF. After the CD is turned OFF, turn the RS signal ON.
3) After turning the RS signal ON, transmit data.
4) After completing the data send, turn OFF the RS signal.
5) If the CD signal turns ON during the data send, continue transmitting data send to the A1SJ71C24. (This occurs when the A1SJ71C24 and the external device start data transmission simultaneously.)
6) Transmit all interrupted data from the external device to the A1SJ71C24 after data send from the A1SJ71C24 is completed.

*1 The time from when the RS signal turns ON until communications start varies with the data transmission speed.
The faster the transmission speed is, the sooner communications will start.

REMARK

When (a) starting or during the data transmission to the A1SJ71C24, and (b) if the DSR(DR) signal of A1SJ71C24 turns OFF or when a DC3 code is received, interrupt data transmission until the DSR signal turns ON or until a DC1 code is received.

(2) A1SJ71C24 is set to " non-priority ".



The following steps describe the operations performed by A1SJ71C24 at every thing. The signal names are of the signals of the A1SJ71C24.

As described in (1), turn ON/OFF the RS signal of the A1SJ71C24 and do data transmission to the external device.

Note that 5) is different.

1) When not transmitting data from the external device to the A1SJ71C24, turn the RS signal OFF.
2) When doing a data send, check the CD signal. If the CD signal is OFF, turn the RS signal ON.
   If the CD signal is ON, wait until it turns OFF. After the CD is turned OFF, turn ON the RS signal.
3) After turning the RS signal ON, transmit data.
4) After completing the data send, turn OFF the RS signal.
5) If the CD signal turns ON during data send, stop the data send. Then, turn the RS signal OFF and perform data receive processing. (This occurs when the A1SJ71C24 and an external device start data transmission simultaneously.)
6) After transmission from the external device is completed, resend all data from the beginning, or transmit data remaining after the send interruption in 5).

*1 Data set at buffer address 110H is not transmitted.

*2 Resend all data from the beginning, or transmit data remaining after the send interruption according to the setting of buffer address 111H.

REMARK

When (a) starting or during the data transmission to the external device and (b) if the DSR(DR) signal of A1SJ71C24 turns OFF or when a DC3 code is received, interrupt data transmission until the DSR signal turns ON or until a DC1 code is received.

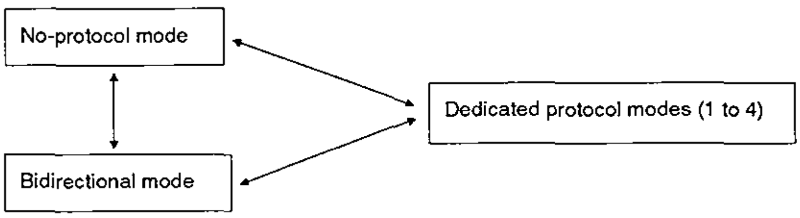
6. SWITCHING THE MODE WHILE THE A1SJ71C24 IS OPERATING

Switching the mode while the A1SJ71C24 is operating (send control protocol switching)

This section should be read to continue data communications with a communicating device if the mode is switched while an A1SJ71C24 is operating.

If the mode is not switched, it is not necessary to read this section.

While an A1SJ71C24 is operating, switching can be done between the following modes.



Mode settings can be switched by the following methods.

(1) Switching the mode using an external device

- Dedicated protocol modes (1 to 4) → Dedicated protocol modes (1 to 4)
  → No-protocol mode *1

(2) Switching the mode using a PC CPU

- Dedicated protocol modes (1 to 4) → Dedicated protocol modes (1 to 4)
  → No-protocol mode
  → Bidirectional mode
- No-protocol mode → Dedicated protocol modes (1 to 4)
  → Bidirectional mode
- Bidirectional mode → Dedicated protocol modes (1 to 4)
  → No-protocol mod

*1 If the mode is switched while the A1SJ71C24 is operating, the READY signal (Xn7) of the A1SJ71C24 goes OFF and is turned ON again.

When it is necessary to switch each set value of the special-applications area (addresses 100H to 11FH) of the A1SJ71C24 buffer, switch a set value at the leading edge of the A1SJ71C24 READY signal (Xn7) just after the signal is turned ON.

It can be switched to the bidirectional mode from a dedicated protocol modes (1 to 4) and data communications can be restarted.

The mode switching timing between the external device and the PC CPU must be adjusted beforehand.

6.1 Precautions When Switching Modes

Precautions to take when (a) switching the mode of an operating A1SJ71C24 and (b) continuing data communications are given below.

(1) Mode setting between an external device and a PC CPU

The following rules must be determined when doing mode switching between an external device and a PC CPU.

(a) In which direction (to/from an external device and a PC CPU) will the mode switching take place?

(b) The timing of the following mode switches must always be determined.

Dedicated protocol modes(1 to 4) → No-protocol/bidirectional modes
No-protocol/bidirectional modes → Dedicated protocol modes(1 to 4)
No-protocol mode → Bidirectional mode
Bidirectional mode → No-protocol mode

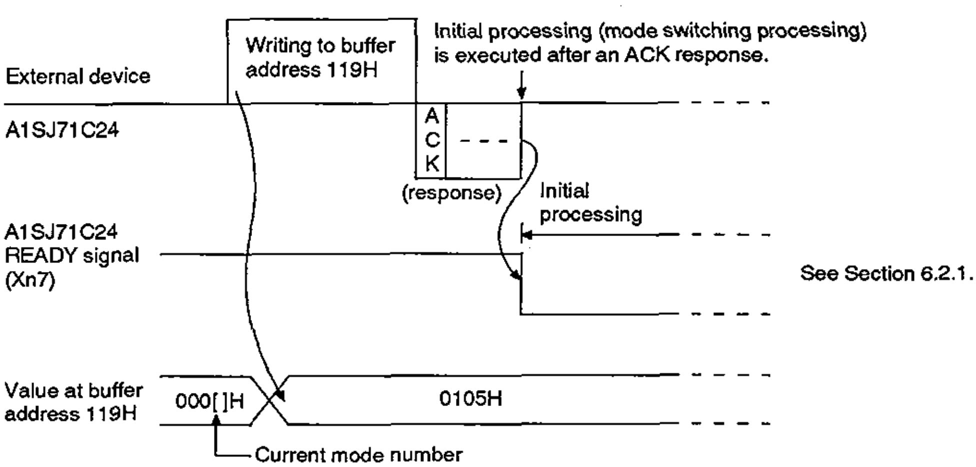
(c) Mode switching message structure when doing mode switching in the no-protocol/bidirectional modes

POINT

Mitsubishi recommends switching the mode from the PC CPU side (see Section 6.2).

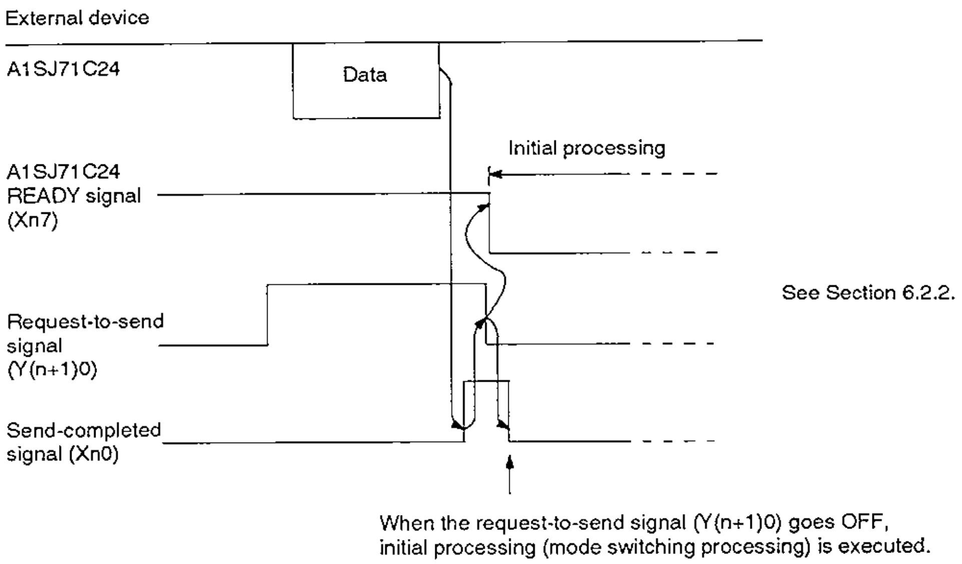
(2) A1SJ71C24 operations when switching modes

(a) If mode switching is requested while communications using a dedicated protocol have not been completed, mode switching processing can only be executed after the A1SJ71C24 has completed data communications (data B - see Section 8.3).

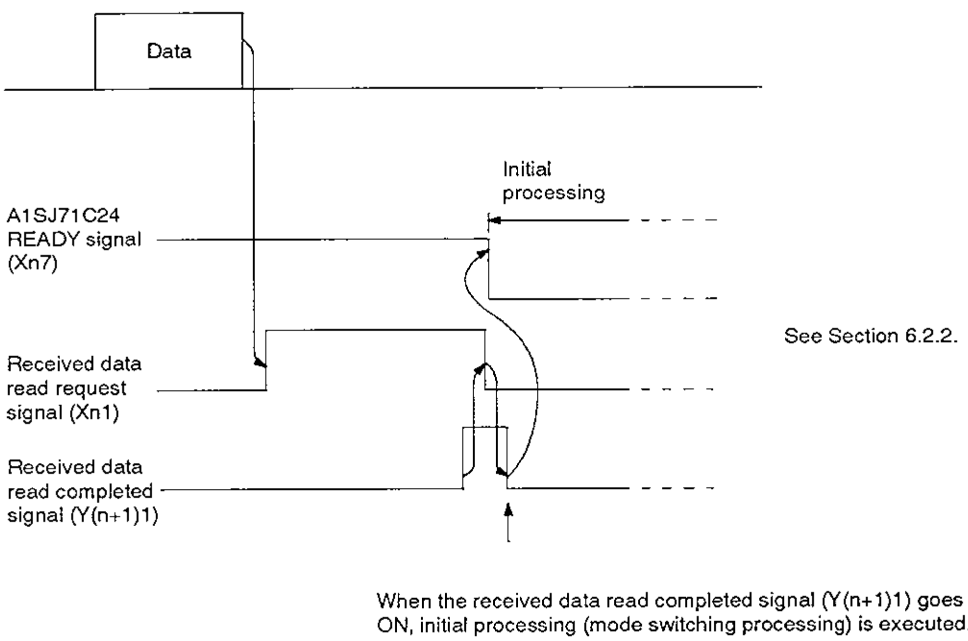


(b) When data communications is done in the no-protocol/bidirectional mode, the A1SJ71C24 switches the mode under the following conditions:

1) If the A1SJ71C24's request-to-send signal (Y(n+1)0) is ON when mode switch processing is executed, that signal is turned OFF.



2) If the A1SJ71C24's received data read request signal (Xn1) is ON when mode switch processing is executed, the received data read completed signal (Y(n+1)1) is turned ON



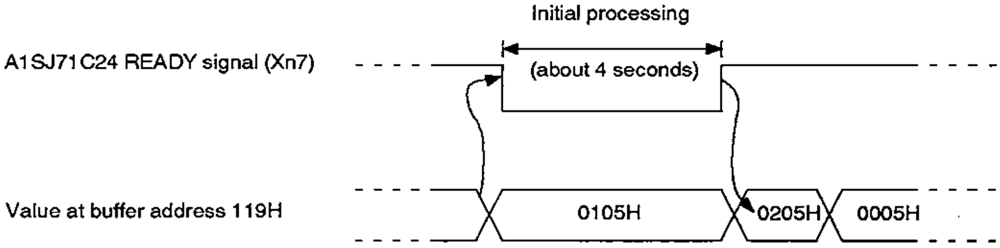
(c) When the mode is switched, the following processing takes place.

1) The value of the special-applications area (buffer addresses 100H to 11FH) of the A1SJ71C24 returns to a default value.

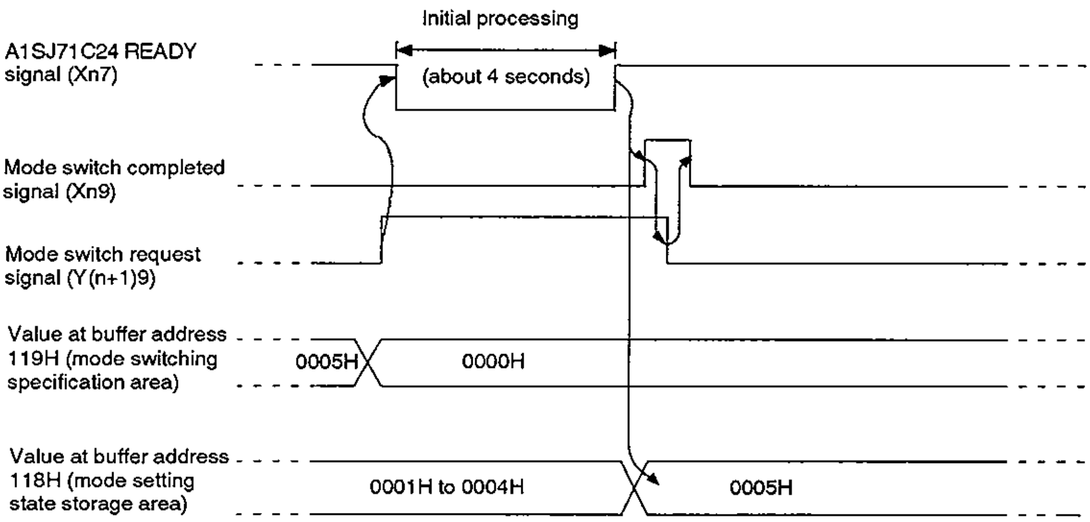
2) During data communications in the no-protocol/bidirectional mode, received data stored in the A1SJ71C24 buffer and OS user area is cleared.

3) The READY signal (Xn7) is turned OFF or ON by the following timing.

- Switching the mode using an external device
  (dedicated protocol modes 1 to 4 ⟶ no-protocol mode)



- Switching the mode using a PC CPU
  (dedicated protocol modes 1 to 4 ⟶ no-protocol mode)



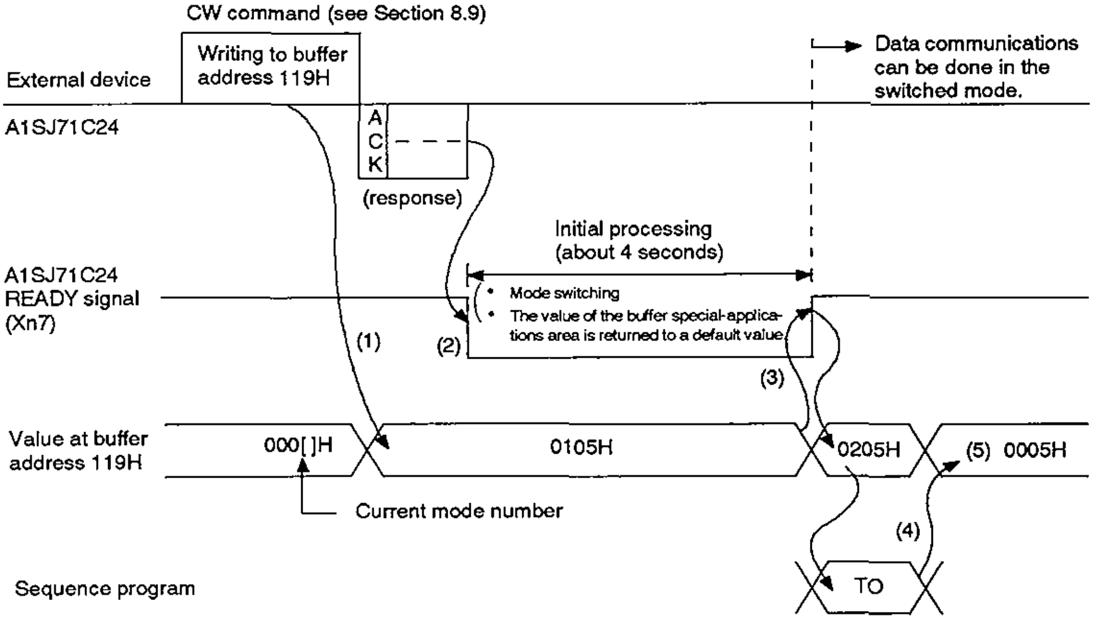
6.2 Mode Switching Methods

6.2.1 Mode switching from an external device

Switching to the no-protocol mode from a dedicated protocol mode (1 to 4) is done by the following method.

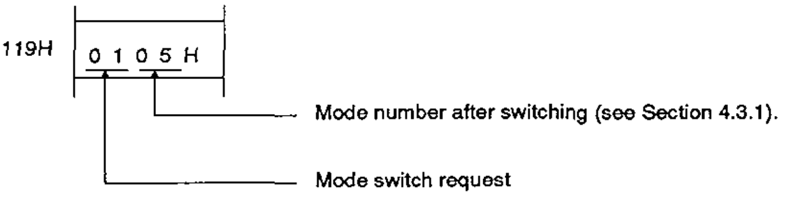
However, the set value of the special-applications area (buffer addresses 100H to 11FH) of the A1SJ71C24 is set at a default value. Data communications must be done in the default value state.

Use a PC CPU to (a) switch to a mode other than the above, or (b) switch the set value in the buffer special-applications area (see Sections 6.1 and 6.2.2).



The operations and processing of the signal timings given in the figure are explained below.

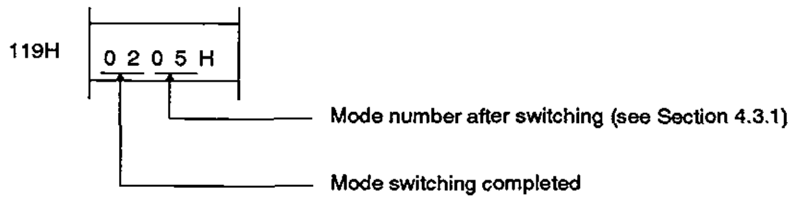
(1) Use a CW command from an external device to write a mode switch request and a mode number in the mode switching specification area (buffer address 119H) of the A1SJ71C24.



(2) After the A1SJ71C24 completes processing of the CW command normally and transmits a response message, the READY signal (Xn7) of the self is turned OFF, and the following mode switching processing is executed.

- The mode of the A1SJ71C24 is switched.
- The value of the special-applications area of the A1SJ71C24 buffer is returned to a default value (excluding the mode switching specification area [buffer address 119H]).

(3) The A1SJ71C24 turns the READY signal (Xn7) of the self ON after completing 2) and switches the value of the higher byte of the mode switching specification area of the buffer to 02H.



(4) After rewriting the value of the higher byte of the mode switching specification area of the A1SJ71C24 buffer to 02H, if the user switches the value of the special-applications area, use a PC CPU to write any desired value to the special-applications area.

If the value of a special-applications area is not switched, the processing of 4 is unnecessary. Execute processing of 5.

(5) Use a PC CPU to read the mode switching specification area of the A1SJ71C24 buffer, set the higher byte to 00H, and write it to the mode switching specification area.

Value in the read mode switching specification area.	02H	05H
Set the higher byte to 00H.	00H	05H

Write it to the mode switching specification area. ↓ To the mode switching specification area

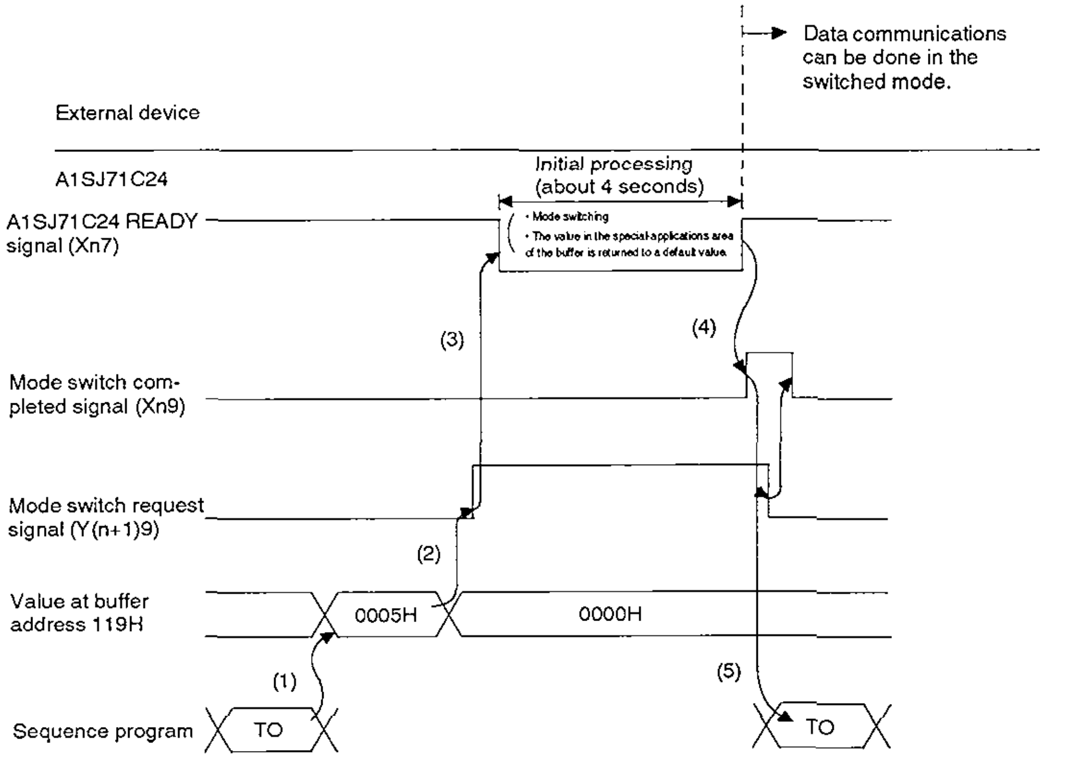
POINTS

(1) Do the following when switching a value in other than the mode switching specification area (buffer address 119H) of the A1SJ71C24 special-applications area during mode switching. After the higher byte value of the mode switching special-applications area becomes 02H, then use the PC CPU to write any desired value at the leading edge of the A1SJ71C24 READY signal (Xn7) just after the signal has turned ON.

(2) The mode of the A1SJ71C24 can be switched even if the PC CPU is in the STOP state.

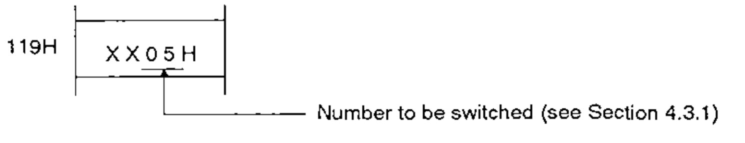
6.2.2 Switching the mode using a PC CPU

(1) This section shows how to switch to a no-protocol/bidirectional mode from a dedicated protocol mode (1 to 4).



The operations and processing of the signal timings given in the figure are explained below.

(a) Use a PC CPU to write the mode number to be switched to the mode switching specification area (buffer address 119H) of the A1SJ71C24.



(b) Use the PC CPU to turn ON the mode switch request signal (Y(n+1)9).

(c) The A1SJ71C24 turns the READY signal (Xn7) of the self OFF and executes the following mode switching processing.

- The mode of the A1SJ71C24 is switched.
- The value of the special-applications area of the A1SJ71C24 buffer is returned to a default value (excluding the mode switching specification area [buffer address 119H]).

(d) After completing 2) above, the A1SJ71C24 turns the READY signal (Xn7) and mode switch completed signal (Xn9) ON.

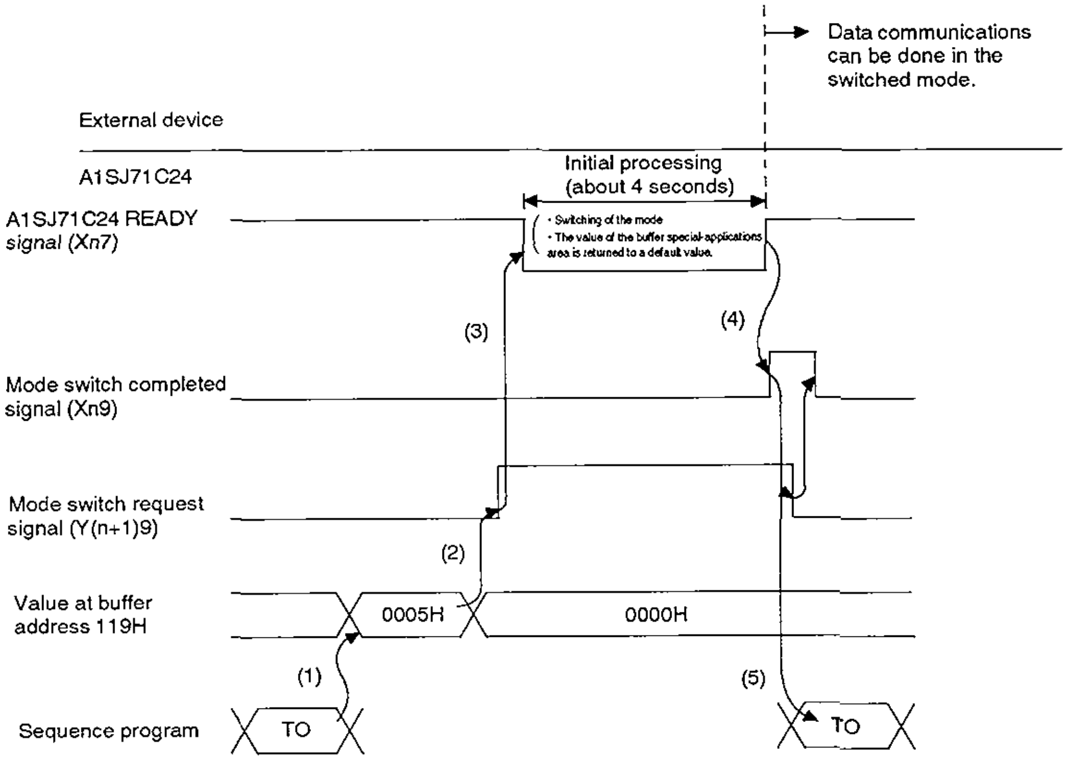
(e) After the mode switch completed signal (Xn9) and the READY signal (Xn7) are turned ON, the PC CPU must turn OFF the mode switch request signal (Y(n+1)9).

If the value is set to other than a default value when the A1SJ71C24 special-applications area does data communications, use a PC CPU to write necessary data to the buffer special-applications area at the leading edge of A1SJ71C24 READY signal (Xn7) immediately after the signal has turned ON.

POINT

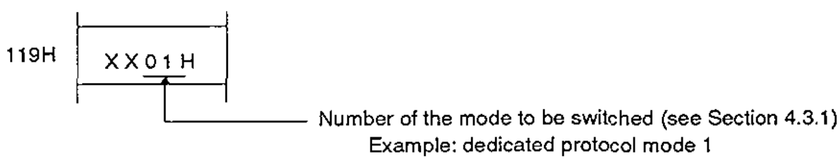
During mode switching, when switching a value in other than the mode switching specification area (buffer address 119H) of the A1SJ71C24 buffer special-applications area, write any desired value at the leading edge of the A1SJ71C24 READY signal (Xn7) just after the signal has turned ON.

(2) This section shows how to switch from a no-protocol/bidirectional mode to a dedicated protocol mode.



The operations and processing of the signals timings given in the figure are explained below.

(a) Use a PC CPU to write the mode number to be switched to the mode switching specification area (buffer address 119H) of the A1SJ71C24.



(b) Use the PC CPU to turn ON the mode switch request signal (Y(n+1)9).

(c) The A1SJ71C24 turns the READY signal (Xn7) of the self OFF and executes the following mode switching processing.

- The mode of the A1SJ71C24 is switched.
- The value of the special-applications area of the A1SJ71C24 buffer is returned to a default value (excluding the mode switching specification area [buffer address 119H]).

(d) After completing 2) above, the A1SJ71C24 turns the READY signal (Xn7) and mode switch completed signal (Xn9) ON.

(e) After the mode switch completed signal (Xn9) and the READY signal (Xn7) are turned ON, the PC CPU must turn OFF the mode switch request signal (Y(n+1)9).

If the value is set to other than a default value when the A1SJ71C24 special-applications area does data communications, use a PC CPU to write necessary data to the buffer special-applications area at the leading edge of A1SJ71C24 READY signal (Xn7) immediately after the signal has turned ON.

POINT

When switching a value other than in the mode switching specification area (buffer address 119H) of the A1SJ71C24 special-applications area when switching the mode, write any desired value at the leading edge of the A1SJ71C24 READY signal (Xn7) just after the signal has turned ON.

7. INITIAL SETTING OF TRANSMISSION CONTROL DATA TO BUFFER MEMORY

The buffer memory has a special applications area for setting transmission control data for communications with external devices (see Section 3.5).

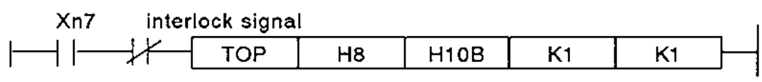
Each transmission data item has a default value. However (depending on the purpose and application of data transmission), using default values not only makes data communications more complicated, but may even preclude them. This section describes the settings of all items in the buffer memory special applications area, shows how to make changes, and gives specific examples. Section 8.14 discusses the special applications area used with the on-demand function of the dedicated protocol.

POINTS

(1) This section only applies to changing preset default values. It does not cover data communications using these default values.

(2) When changing a setting (except for the error LED display area and the error LED turn-OFF request area) first turn the power supply OFF and back ON or else reset the PC CPU. Change the setting after the A1SJ71C24 READY signal (Xn7) is turned ON, as shown below.

Example: How to disable the RS-232C CD terminal check function



(3) Buffer memory addresses 10EH and 11DH to 11FH are reserved for the system only. Writing data to these addresses precludes normal operation of the A1SJ71C24.

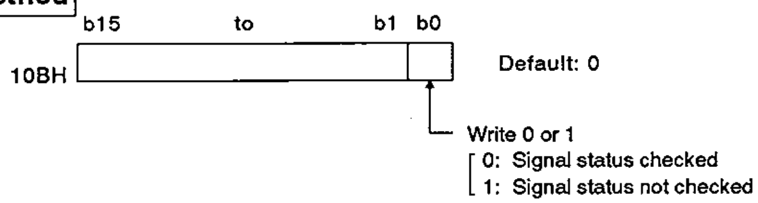
7.1 Setting RS-232C CD Terminal Check Enable/Disable

Setting this RS-232C CD terminal check function to enable or disable determines whether or not the A1SJ71C24 checks the ON/OFF status of the CD signal (receive carrier detection signal).

Disabling the RS-232C CD terminal check function.

If a "1" is written to buffer memory address 10BH, the A1SJ71C24 does not check the ON/OFF status of the CD signal. It operates as if the CD signal were ON.

Setting method



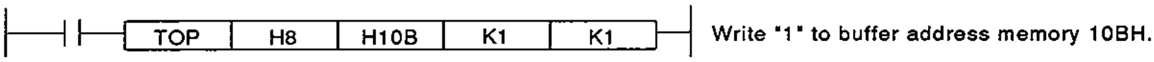
POINT

Set bits b1 to b15 of address 10BH to either 0 or 1.
(The A1SJ71C24 will ignore the settings.)

Example

How to disable the RS-232C CD terminal check function (A1SJ71C24 I/O addresses 80 to 9F).

(Sequence Program)



POINT

When the RS-232C is set to use half-duplex transmission (see Section 7.2), set the CD terminal check to "Enabled". Section 4.5.2 explains the connecting procedure.

If the CD terminal check is set to "Disabled", the transmission method is automatically set to full-duplex transmission.

7.2 Setting the Transmission Method for RS-232C

Set the transmission method used with the RS-232C interface which connects the A1SJ71C24 to the external device. Both half-duplex and full-duplex transmissions can be used for setting. If the half-duplex transmission is used, the following settings should be made:

- Whether or not the A1SJ71C24 continues or stops transmission when the A1SJ71C24 and the external device have begun sending data to each other at the same time. (Priority/non-priority setting at simultaneous transmission)
- Whether or not the A1SJ71C24 transmits data again from the beginning or from the point where transmission stopped when it restarts transmission. (Transmission method when the transmission restarts.)

Set the transmission method which conforms to the specifications of the connected device.

POINTS

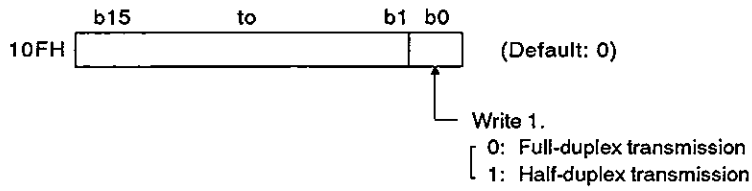
- When full-duplex transmission is used, settings with buffer memory addresses 10FH, 110H, and 111H are not required.
- Section 5.2 gives settings required for half-duplex transmission.
- When using half-duplex transmission, set the RS-232C CD terminal check to "Enabled" (see Section 7.1).

7.2.1 Setting priority of transmission to the A1SJ71C24 using half-duplex transmission

The following shows how to set the A1SJ71C24 to continue transmission when the A1SJ71C24 and an external device (using half-duplex transmission) have begun sending data to each other simultaneously.

Setting method

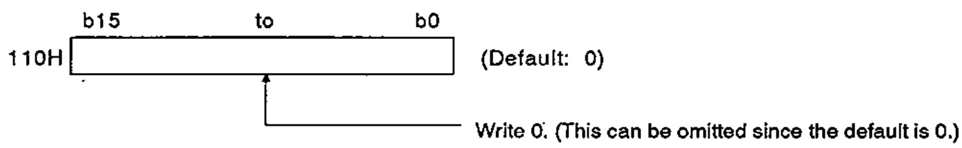
(1) Transmission method



POINT

- Set bits b1 to b15 of address 10FH to either 0 or 1. (The A1SJ71C24 will ignore the settings.)

(2) Priority setting when transmission has begun at the same time



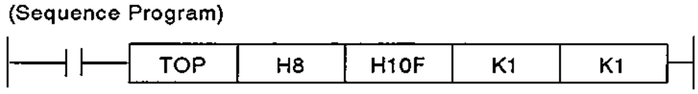
POINT

If the priority of transmission is set, setting to buffer memory address 111H is not required.

Example

The CD terminal check is set to "Enabled". Half-duplex transmission is used and the priority of transmission is set. (A1SJ71C24 I/O addresses: 80 to 9F)

(Sequence Program)



Write "1" to buffer memory address 10FH.

Leave the setting of buffer memory addresses 10BH and 110H for defaults.

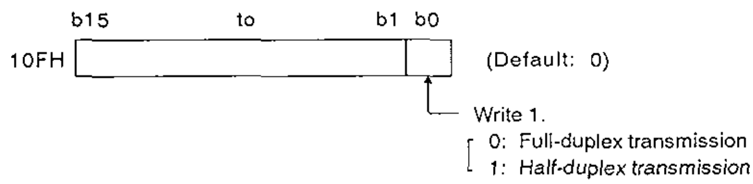
7.2.2 Setting non-priority of transmission to the A1SJ71C24 with the half-duplex transmission

The following shows how to set the A1SJ71C24 to discontinue transmission when the A1SJ71C24 and an external device (using half-duplex transmission) have begun transmitting data to each other simultaneously.

(1) Setting "half-duplex transmission", "non-priority", and "not resend":

Procedure

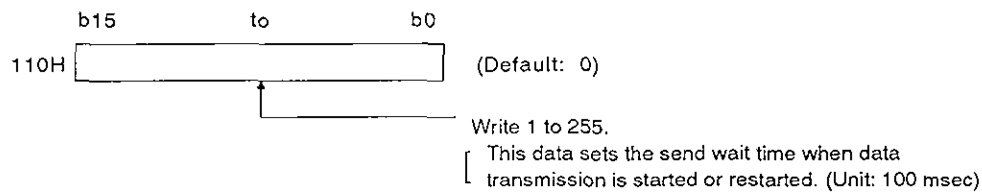
(1) Transmission method



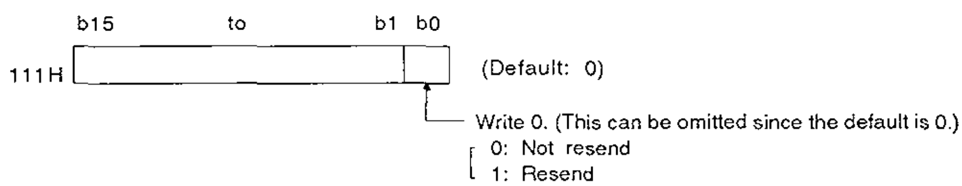
POINT

- Set bits b1 to b15 of address 10FH to either 0 or 1. (The A1SJ71C24 will ignore the settings.)

(2) Priority setting when transmission has begun simultaneously



(3) Transmission method when data transmission is restarted



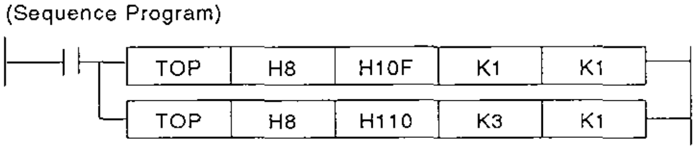
POINT

Set bits b1 to b15 of address 111H either to 0 or 1. (The A1SJ71C24 will ignore the settings.)

Example

The CD terminal check is set to "Enabled". Half-duplex transmission is used and the non-priority of transmission and "not resend" are set. (Send wait time: 300 msec) (A1SJ71C24 I/O addresses: 80 to 9F)

(Sequence Program)



Write "1" to buffer memory address 10FH.

Write "3" to buffer memory address 110H.

Leave the setting of buffer memory addresses 10BH and 111H for defaults.

(2) To set "half-duplex transmission", "non-priority", and resend.

Setting method

(1) Transmission method

b15 to b1 b0

10FH (Default: 0)

Write 1.
- 0: Full-duplex transmission
- 1: Half-duplex transmission

POINT

Set bits b1 to b15 of address 10FH to either 0 or 1. (The A1SJ71C24 will ignore the settings.)

(2) Priority setting when transmission has begun simultaneously

b15 to b0

110H (Default: 0)

Write 1 to 255.
This data sets the transmission wait time when data transmission is started or restarted. (Unit: 100 msec)

(3) Transmission method when data transmission is restarted

b15 to b1 b0

111H (Default: 0)

Write 0. (This can be omitted since the default is 0.)
- 0: Not resend
- 1: Resend

POINT

Set bits b1 to b15 of address 111H to either 0 or 1. (The A1SJ71C24 will ignore the settings.)

Example

The CD terminal check is set to "Enabled". Half-duplex transmission is used and the non-priority of transmission and "resend" are set. (Send wait time: 100 msec) (A1SJ71C24 I/O addresses: 80 to 9F)

(Sequence Program)

TOP	H8	H10F	K1	K1	Write "1" to buffer memory address 10FH.
TOP	H8	H110	K10	K1	Write "10" to buffer memory address 110H.
TOP	H8	H111	K1	K1	Write "1" to buffer memory address 111H.

Leave the setting of buffer memory address 10BH for default.

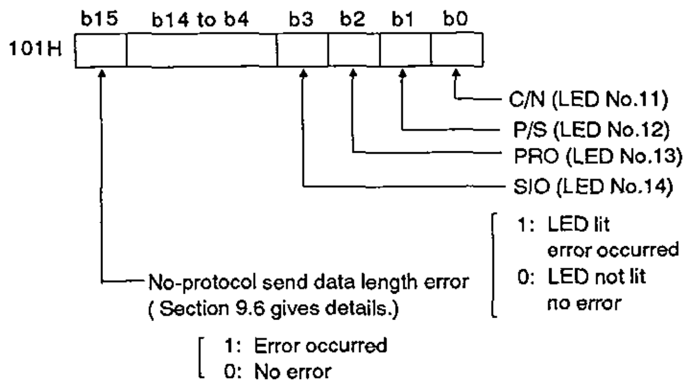
7.3 Reading Transmission Error Data

This section explains the contents of the buffer memory area where the ON/OFF status of the error LEDs are stored. It also shows how to turn LEDS which are lit OFF.

7.3.1 Reading the error LED display status

(1) Error LED display status storage area

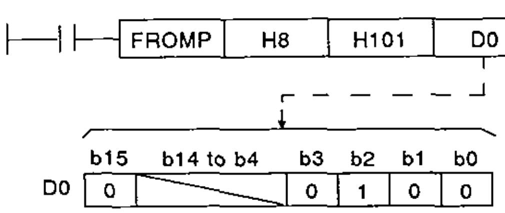
The ON/OFF status of the error LEDs are stored in address 101H of the buffer memory (see below).



(2) Program example to read the error LED display status storage area

This gives an example of a program using the sequence program [FROM] to read the error LED display ON/OFF status stored in buffer memory address 101H.

Program example to read the error LED display status storage area (A1SJ71C24 I/O addresses 80 to 9F)



Read the contents of the error LED display status storage area to address D0

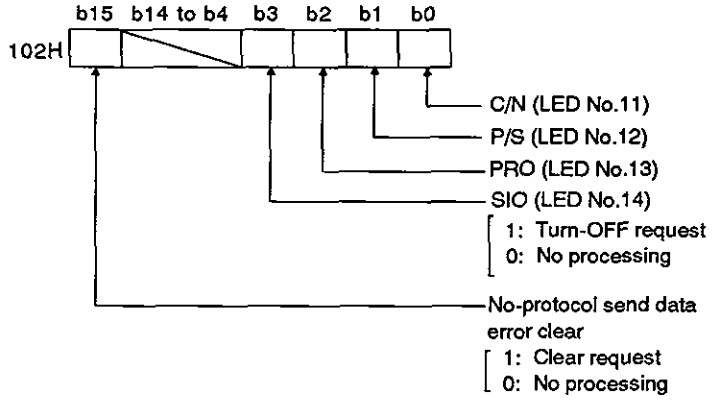
...This shows that the PRO (LED No.14) is ON. This means an RS-232C protocol error has occurred.

7.3.2 Turning OFF error LEDs

When an error LED turns ON, it stays ON (lit) even when the cause of the error has been eliminated.

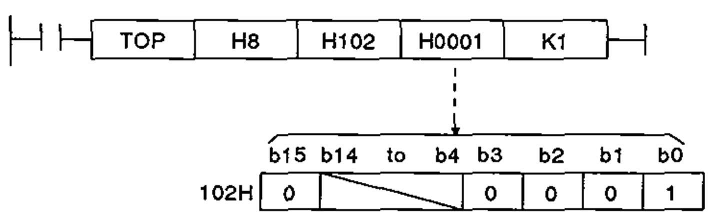
To turn OFF the lit LED, "1" must be written to the appropriate bit of address 102H of the buffer memory, using the sequence program TO instruction.

(1) Error LED turn-OFF request area



(2) Program example to turn OFF error LEDs

A sequence program example to turn OFF LED C/N (LED No.12) is given below.



POINTS

(1) The LED turn-OFF request is only valid when it is written.

(2) Relevant data in the error LED display status storage area at address 101H is cleared when the LED turn-OFF request is made. Data at address 102H remains as written.

(3) If the error data has not been cleared after the LED turn-OFF request is made, the error LED will go ON again.

7.4 Settings in the No-Protocol Mode

This section describes setting methods and gives no-protocol mode examples.

7.4.1 Setting the no-protocol mode receive-completed code (for receive with variable-length data)

How to set and modify the receive-completed code and the sequence program for the receive processing with variable-length data are shown below.

Setting method

	b15 to b8	b7 to b0	
Buffer memory address 100H	0 0		Default 0D0AH (CR, LF)

Enter the required completed code
Always write 00H to the higher 8 bits
} When the completed code is set.

POINTS

(1) The completed code can be set to any value which makes 1 byte in the range of 00H to FFH. Since the default value setting is 0D0AH, when the CR and LF codes are received during the data receive, the read request is transmitted to the sequence program (Xn1 is ON). If the default setting has been changed, when a modified completed code is received during the data receive, the read request is transmitted to the sequence program.

(2) If the length of data to complete data receive is also set, the read request for the received data is transmitted when the completed code or the set length of data (whichever comes first) is received. (Xn1 is ON)

(3) If the completed code is not set, set buffer memory address 100H to FFFFH. This enables only the setting of data length to complete receive, and the read of received data by fixed data length is enabled.

Example

To set the end code to ETX (03H) (A1SJ71C24 I/O addresses 80 to 9F)

(Sequence Program)

TOP	H8	H100	H0003	K1

Write the ASCII code for ETX (03H) to buffer memory address 100H

7.4.2 Specifying no-protocol receive completion data length (fixed length)

How to complete the data receive and set the data length are given below along with a sequence program example.

Setting method

	b15 to b0
Buffer memory address 108H	

Write the amount of received data (default: 127 words)

POINTS

(1) Set the length of data to complete the data receive in the following ranges:

Length of data received ≤ no-protocol mode buffer size (when word units are set)

Length of data received ≤ no-protocol mode buffer size x 2 (when byte units are set)

If the received data length is larger than the no-protocol mode buffer size, then it is automatically set equal to the no-protocol mode buffer size.

(2) Section 7.4.3 describes the selection of a word or byte unit for the data length to complete data receive.

(3) If the receive-completed code is set, the read request for the received data is transmitted when the completed code or the set data length (whichever comes first) is received. (Xn1 is ON)

(4) To read the received data by fixed length without setting the completed code, do the following setting:

Write FFFFH.

	b15 to b8	b7 to b0
Buffer memory address 100H	F F	F F
Buffer memory address 108H		

Write the length of received data (default : 127 words)

Example

To set the fixed length at which data receive is complete to 15 words in the case of the read of received data only by fixed length (A1SJ71C24 I/O addresses 80 to 9F)

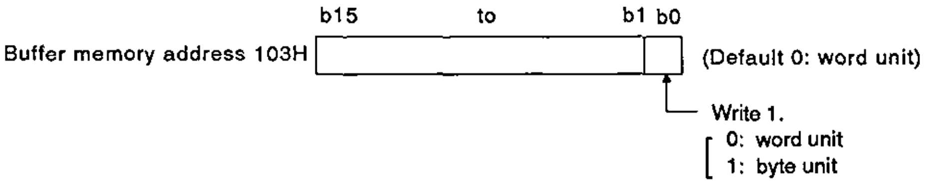
(Sequence Program)

TOP	H8	H100	HFFFF	K1	To specify the fixed length, write HFFFF to buffer memory address 100H.
TOP	H8	H108	K15	K1	Write "15" to buffer memory address 108H.

7.4.3 Setting a word or byte unit in the no-protocol mode

This section shows how to set the word or byte unit for data communications and gives an example.

Setting method



POINTS

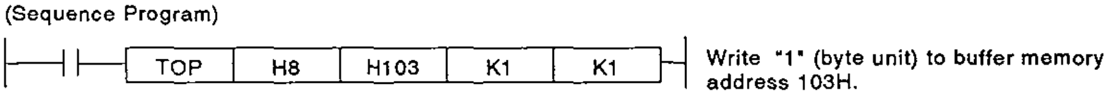
(1) The word or byte unit set here only applies to comunications data in the no-protocol/bidirectional mode and on-demand data using a dedicated protocol.

(2) Set bits b1 to b15 of address 103H to either 0 or 1. (The A1SJ71C24 will ignore the settings.)

Example

To set the byte unit (A1SJ71C24 I/O addresses 80 to 9F)

(Sequence Program)

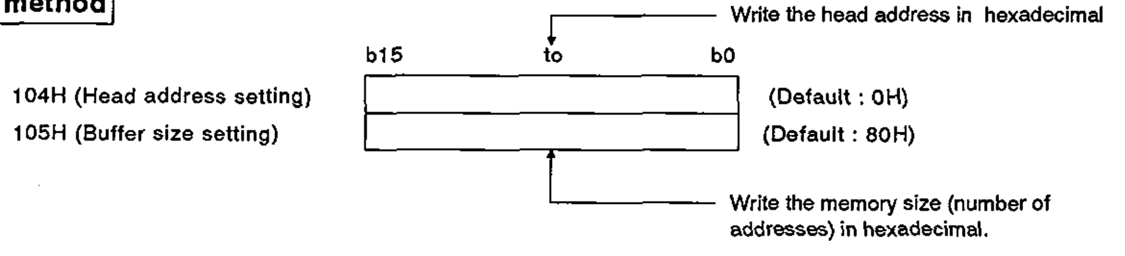


7.4.4 Setting a buffer memory area for no-protocol send

This section describes how to set the A1SJ71C24 buffer memory area to store data transmitted from the PC CPU to an external device in the no-protocol mode and gives an example.

When the bidirectional mode setting area (address 112H) is set to "1", this memory area is set for bidirectional mode transmission.

Setting method



POINTS

(1) Buffer memory addresses 100H to 11FH are for the special applications area and should not be set.

(2) When other kinds of devices are also used, make sure that the specified range does not overlap the no-protocol receive area or the on-demand data area.

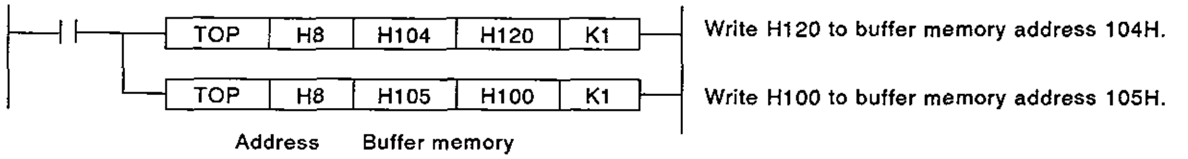
(3) Buffer memory address 105H should include the storage area of the no-protocol send data length.

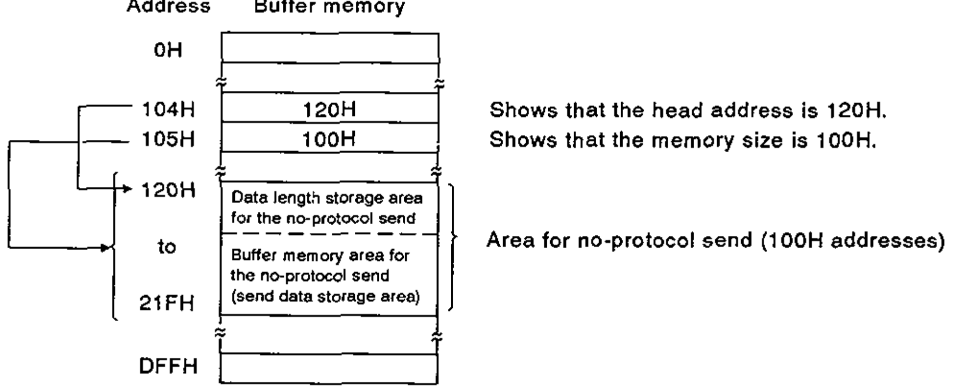
(4) If any range except the user area is set, the A1SJ71C24 will execute operations with defaults including the areas mentioned in (2) above.

Example

To set the head address to 120H and the memory size to 100H (A1SJ71C24 I/O addresses 80 to 9F).

Sequence Program



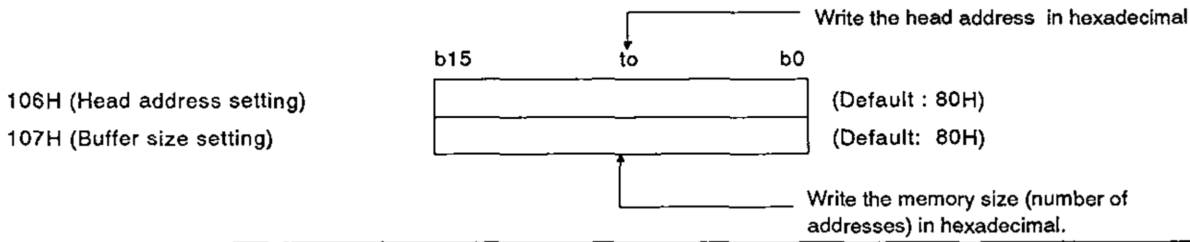


7.4.5 Setting a buffer memory area for no-protocol receive

This section shows how to set the A1SJ71C24 buffer memory area to store data the PC CPU received from the external device in the no-protocol mode. An example is also given.

When the bidirectional mode setting area (address 112H) is set to "1", this memory area is set for bidirectional mode transmission.

Setting method



POINTS

(1) Buffer memory addresses 100H to 11FH are for the special application area and should not be set.

(2) Make sure that the specified range does not overlap the no-protocol mode send area or the on-demand data area.

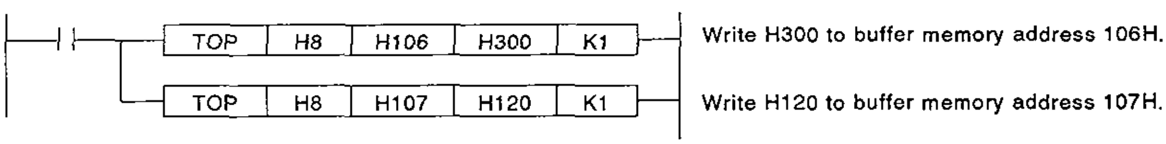
(3) Buffer memory address 107H should include the storage area of the no-protocol receive data length.

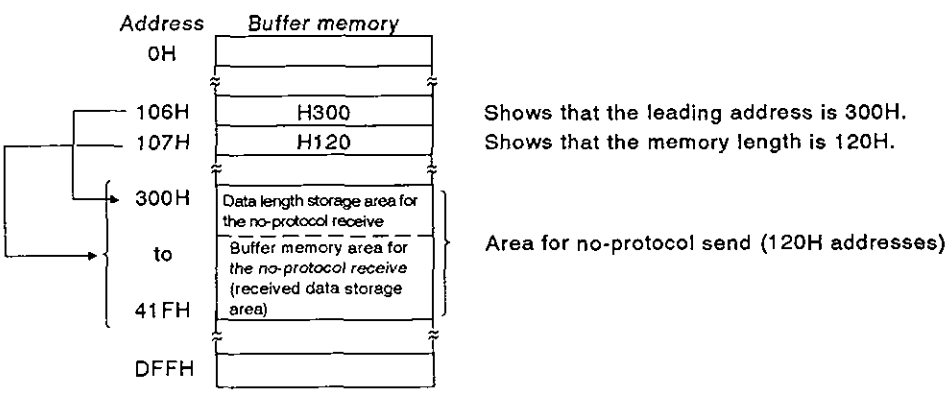
(4) If any range except the user area is set, the A1SJ71C24 will execute operations with defaults including the areas mentioned in (2) above.

Example

To set the head address to 300H and the memory size to 120H (A1SJ71C24 I/O addresses 80 to 9F).

(Sequence Program)





7.5 Settings in the Bidirectional Mode

This section describes how to set items in the bidirectional mode and gives examples.

The defaults set with the buffer memory section are for the no-protocol mode. When the interface mentioned in (1) is used in the no-protocol mode, all settings mentioned in this section are not necessary.

(1) Setting the bidirectional mode (address 112H)

Set the switch to "1".

(2) Setting the time-out check time (address 113H)

Set the time-out check time which specifies the time from the beginning of data send to a computer connected through the bidirectional mode interface until the reception of the response message (see the figure in Section 10.5.1).

(3) Valid/invalid setting of data at simultaneous transmission (address 114H)

Set the data transmitted and received by the A1SJ71C24 to valid/invalid when a computer and the A1SJ71C24 begin simultaneously full-duplex send in the bidirectional mode (see Section 10.6).

(4) Setting the check sum enable/disable (address 115H)

Set whether the check sum code is added or not added to the message when transmitted between the A1SJ71C24 and a computer in the bidirectional mode. (see Section 10.5.2 (4)).

This setting is unrelated to the check sum setting (for dedicated protocol) with SW12 of the A1SJ71C24.

POINT

Sections 7.4.3 to 7.4.5 give the settings of the following areas used in the bidirectional mode. (Since the explanations in Sections 7.4.3 to 7.4.5 are for the no-protocol mode, change the mode from non-protocol to bidirectional when referring to these sections.)

- Bidirectional word/byte setting area: . . . . . Section 7.4.3
- Bidirectional send area: . . . . Section 7.4.4
- Bidirectional receive area: . . . . Section 7.4.5

Setting method

(1) Bidirectional mode

Buffer memory address 112H	b15 to b0	(Default: 0)

Write 1.
0: No-protocol mode
1: Bidirectional mode

POINT

When the bidirectional mode is set, settings with buffer memory addresses 113H to 115H are valid.

(2) Time-out check time

Buffer memory address 113H	b15 to b0	(Default: 0H)

Write 0H to FFFFH.
0H: Time-out check disabled (infinite wait)
1H to FFFFH: Time-out check enabled
(Set value is processed as 1 to 65535 which is the time-out check time. Time-out check is executed during the response message wait. (Unit: 100 msec))

(3) Data valid/invalid at simultaneous transmission

Buffer memory address 114H	b16 to b8	b7 to b0	(Default: 0000H)

b7 to b0: Write 1 or 0.
0: Received data valid:
The ACK code is transmitted after receiving data.
1: Received data invalid:
Received data is ignored.

b16 to b8: Write 1 or 0.
0: Send data valid:
Waits for the response message after sending data
1: Send data invalid:
Data send error occurs and the operation ends.

(4) Check sum enable/disable

Buffer memory address 115H	b15 to b0	(Default: 0)

Write 1 or 0.
0: Check sum enable added.
1: Check sum disabled not added.

Setting method

(1) Setting the bidirectional mode with the following conditions (A1SJ71C24 I/O addresses: 80 to 9F)

1) Set the bidirectional mode.

2) Set the time-out check time to 2 seconds. The setting value is 20 (14H).

3) Set the send data to "invalid" and the received data to "valid" for simultaneous transmission.

4) Set the check sum to "disable"

(Sequence Program)

TOP	H8	H112	K1	K1	Write "1" to buffer memory address 112H.
TOP	H8	H113	H14	K1	Write H14 to buffer memory address 113H.
TOP	H8	H114	H100	K1	Write H100 to buffer memory address 114H.
TOP	H8	H115	K1	K1	Write "1" to buffer memory address 115H.

(2) Setting the bidirectional mode with the following conditions (A1SJ71C24 I/O addresses: 110 to 12F)

1) Set the bidirectional mode.

2) Set the time-out check time to "infinite".

3) Set the send data to "valid" and the received data to "valid" for simultaneous transmission.

4) Set the check sum to "enable".

(Sequence Program)

TOP	H11	H112	K1	K1	Write "1" to buffer memory address 112H.

Leave settings of buffer memory addresses 113H for 115H for defaults.

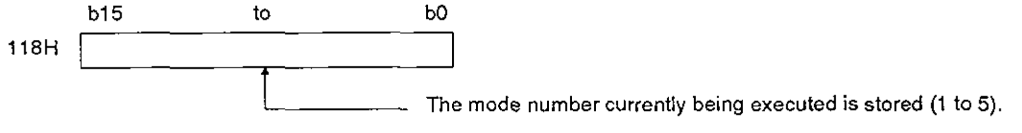
7.6 Mode Switching Setting

This Section shows how to specify a setting item during mode switching and a gives a sample specification.

7.6.1 Reading the mode setting status

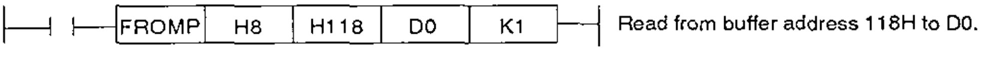
The method for reading the mode number currently being executed is given below.

Specification method



Sample read

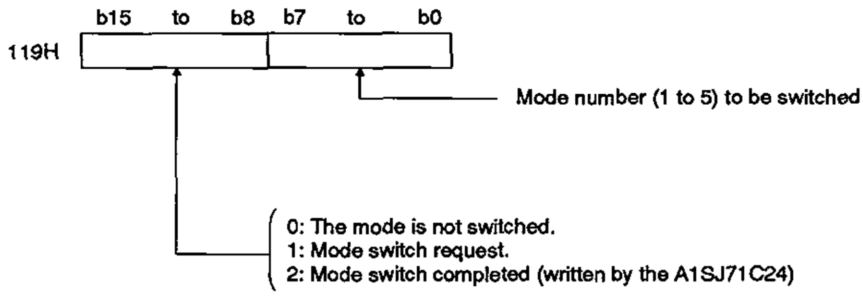
Sample program for reading the mode number currently being executed
(I/O addresses 80 to 9F of the A1SJ71C24)



7.6.2 Mode switching specification setting

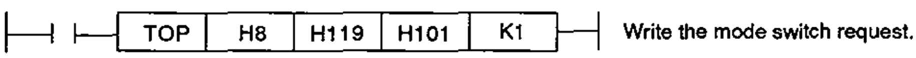
This section shows how to specify mode switching and gives a sample sequence program.

Specification method



Sample specification

Mode switching from a PC CPU (No-protocol - dedicated protocol mode 1)
(I/O addresses 80 to 9F of the A1SJ71C24)



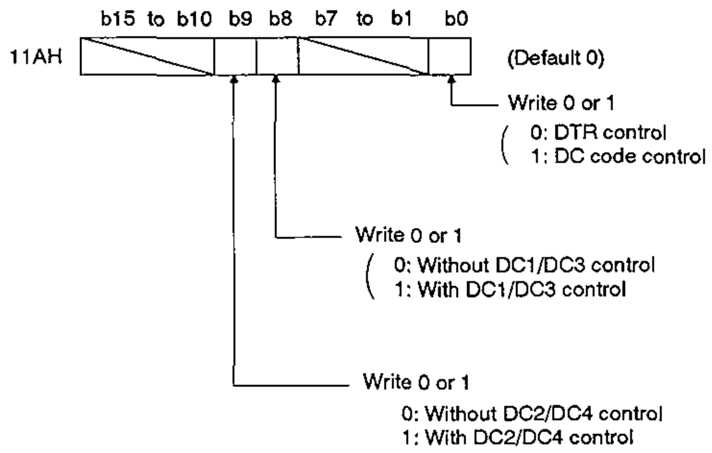
7.7 Send Control Setting

This section shows how to specify a setting item during send control and a gives a sample specification.

7.7.1 Send control setting

This section shows how to specify send control and gives a sample sequence program.

Specification method



POINT

To change the send control method, make sure that communications is not being done with a sequence program (I/O signals (Xn0), (Xn1), Y(n+1)0, (Y(n+1)1) are OFF).

Sample specification

When 'with DC1/DC3 control' is selected (I/O addresses 80 to 9F of the A1SJ71C24)

(Sequence program)

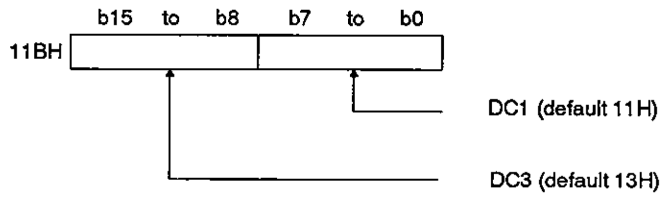
TOP	H8	H11A	H0101	K1

Write H101 to buffer address 11AH.

7.7.2 DC1/DC3 setting

This section shows how to specify the setting and switching of DC1/DC3 code and gives a sample sequence program specification.

Specification method



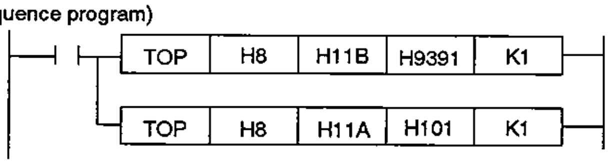
POINT

To change the DC1/DC3, set a byte of code at any value between 00H and FFH.

Sample specification

When DC1 is switched to 91H, and DC3 is switched to 93H
(I/O addresses 80 to 9F of the A1SJ71C24)

(Sequence program)



Write DC1 91H and DC3 93H to buffer address 11BH.
Write 101H to buffer address 11AH.

POINT

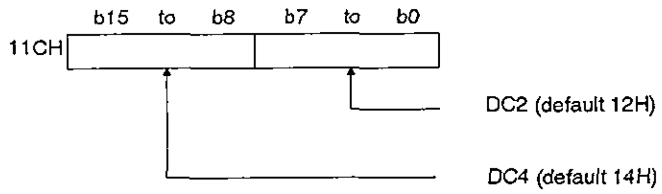
When switching DC1/DC3 from a default value, switch the value of buffer address 11BH.

Make sure that 'with DC1/DC3 control' is specified at buffer address 11AH.

7.7.3 Setting of DC2/DC4

This section shows how to specify the setting and switching of DC2/DC4 and gives a sample sequence program specification.

Specification method



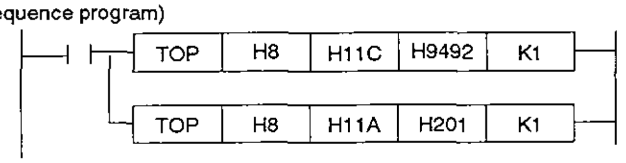
POINT

To change the DC2/DC4, set a byte of code at any value between 00H and FFH.

Sample specification

When DC2 is switched to 92H, and DC4 is switched to 94H
(I/O addresses 80 to 9F of the A1SJ71C24)

(Sequence program)



Write DC2 92H and DC4 94H to buffer address 11CH.
Write 201H to buffer address 11AH.

POINT

When switching DC2/DC4 from a default value, switch the value of buffer address 11CH.

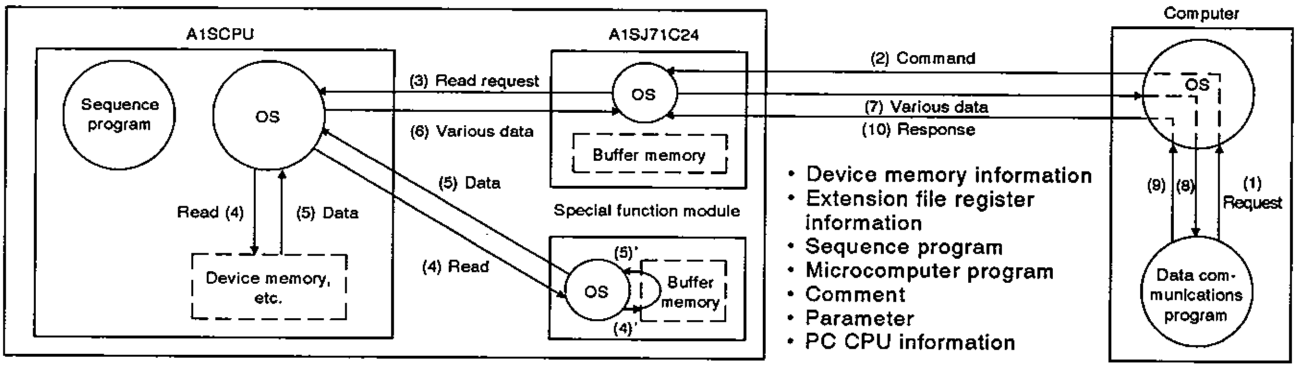
And, make sure that 'with DC2/DC4 control' is specified at buffer address 11AH.

8. COMMUNICATIONS USING DEDICATED PROTOCOLS

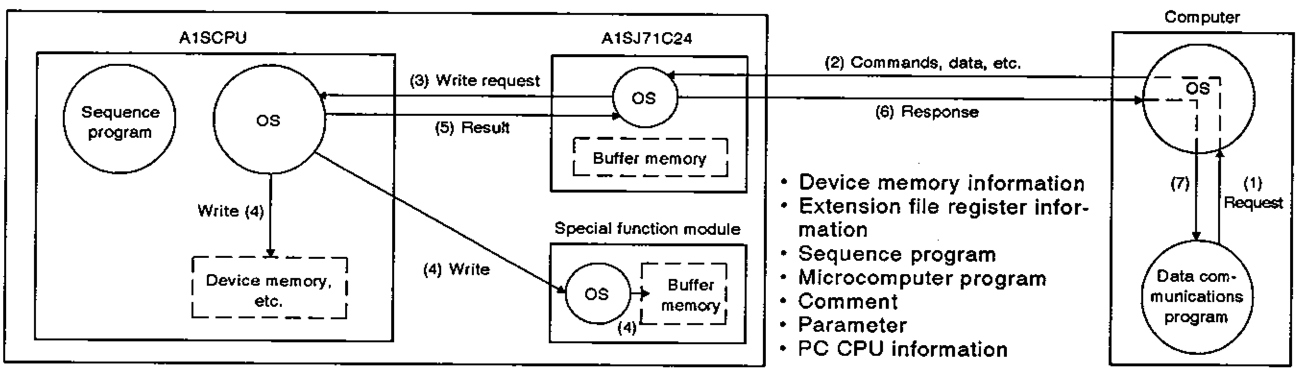
This chapter explains the details and methods of specifying control protocols 1 to 4 along with examples.

8.1 Data Flow in Communications with Dedicated Protocols

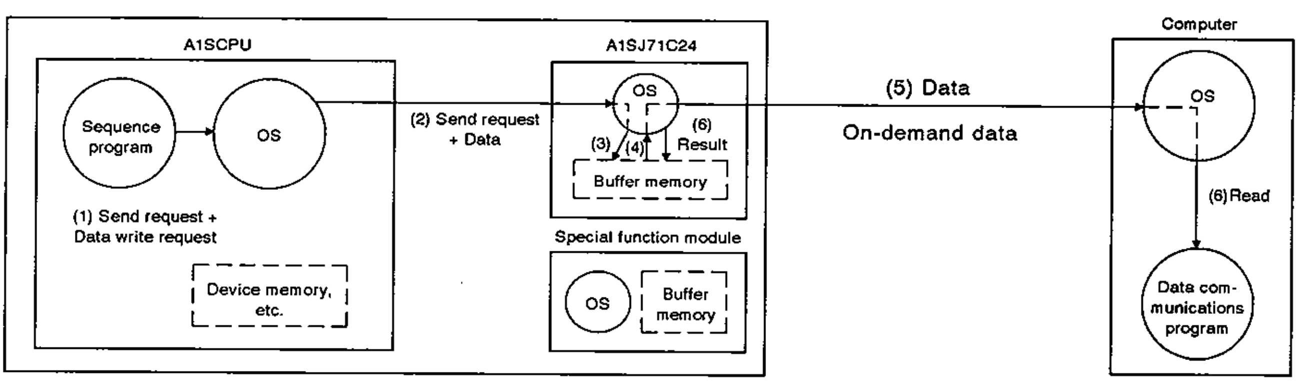
(1) The computer reads data from the A1SCPU



(2) The computer sends data to the A1SCPU



(3) The A1SCPU sends data to the computer



REMARK

The OS (operating system) shown in the above illustrations is the software that uses resources such as the PC CPU, memory, terminals, files, and network efficiently.

In this manual, this software is described as the system program or system.

8.2 *Programming Hints*

8.2.1 To write data to the special use area in buffer memory

(1) Buffer memory is not backed up by a battery.

All data in buffer memory is set to the default values when power is turned ON or when the PC CPU is reset. Data changed from the default values must be written to the buffer memory whenever the power is turned ON or the CPU is reset.

(2) Only TO instruction can be used to write data to the special use area (100H to 11FH). If data is written to the buffer memory using the command in a computer program, the A1SJ71C24 will not operate correctly. Never try to write data using a computer program.

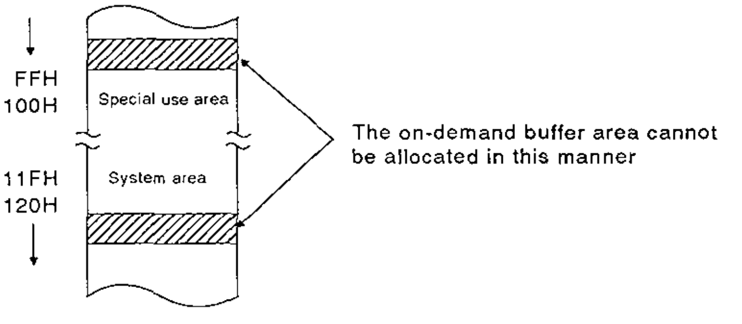
(3) If the following functions are used in combination with the dedicated protocol, make sure to allocate the user area in buffer memory so that the same area will not be used by different functions.

If the same area is allocated to different functions, the data in this area is rewritten and communications will not be correctly executed.

- No-protocol mode transmission or bidirectional mode transmission
- No-protocol mode receive or bidirectional mode receive
- Buffer memory read/write (CR/CW command) function
- On-demand function

The memory areas preceding and following the special use area cannot be allocated as a single area. The areas 0H to FFH and 120H to DFFH must be recognized as independent areas.

Example:



(4) If the designation is made to process the send/receive data in the no-protocol mode or bidirectional mode in units of words or bytes, the on-demand data is processed in the same designated unit.

8.2.2 A1SCPU operation during data communications

(1) A1SCPU scan time

In response to the access request from the A1SJ71C24, the A1SCPU processes only a single request in each END processing while the A1S CPU is running.

Therefore, the scan time is extended by the time used for processing.

For intervening and processing times required for communications between the A1SJ71C24 and A1SCPU, see Appendix 5.

Scan time is extended approximately 0.2 msec when the A1SJ71C24 is loaded, even if the A1SCPU is not linked.

(2) Simultaneous access

Because the A1SCPU executes only a single processing in END processing, if the A1SCPU is accessed by more than one A1SJ71C24, access to the A1SCPU is suspended until other processing is completed. Thus, the number of times scanning is done is increased.

8.2.3 Precautions during data communications

(1) The conditions under which the A1SJ71C24 transmission sequence is initialized are as follows:

- The power supply is turned ON or the PC CPU is reset with the reset switch.
- Data communications is completed normally.
- The control code EOT or CL is received.
- The NAK control code is received.
- During full-duplex communications through the RS-232C interface, the CD signal is turned OFF.

(The ON/OFF status of the CD signal is ignored if the CD terminal check function is disabled.)

(2) NAK response from the A1SJ71C24

The NAK response is given from the A1SJ71C24 to the computer using the dedicated protocol if an error is detected. Therefore, the NAK response may be output even while the computer is sending data in the full-duplex communications mode.

(3) Data link error processing

The A1SJ71C24 enters the standby state (see Section 3.4 I/O list for A1SCPU) if a data link error occurs during data communications with a A1SCPU (the A1SCPU number being other than FFH) on MELSEC-NET/B.

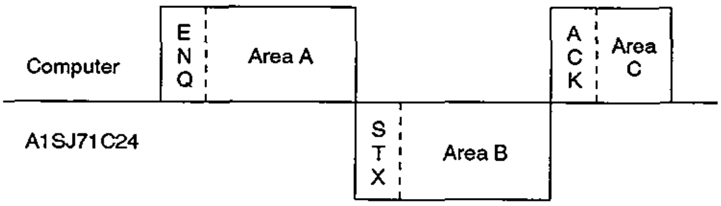
If an error is detected by the computer when executing the time check, send a clear command (EOT or CL, see Section 8.4.5 (1)) to initialize the transmission sequence.

(4) Sending a command from the computer

When sending a command from the computer to the A1SJ71C24 using the dedicated protocol, send the command only after the data communications called by the preceding command is completed.

8.3 Basics of Dedicated Protocol Control Procedures

(1) Reading data by the computer from the A1SJ71C24



(a) Areas A and C indicate transmission from the external device to the A1SJ71C24.

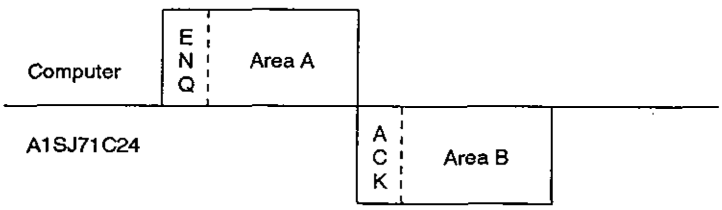
(b) Area B indicates transmission from the A1SJ71C24 to the external device.

(c) Computer programs are created so that all data is transmitted from left to right.

(Example: In area A, data is transmitted to the right after the ENQ signal.)

(d) Area C of the program completes data communications (whether communications are being carried out or not) and permits the next data communications to be carried out.
When area C data is transmitted, it is not processed by the A1SJ71C24.

(2) Writing data by the computer to the A1SJ71C24



(a) Area A indicates transmission from the external device to the A1SJ71C24.

(b) Area B indicates transmission from the A1SJ71C24 to the external device.

(c) Computer programs are created so that all data is transmitted from left to right.

(Example: In Area A, data is transmitted to the right after the ENQ signal.)

8.4 Basic Formats of Dedicated Protocol

There are 4 formats of control protocol. These control formats are selected by the mode setting switch (see Section 4.3.1). The differences between the control formats (based on format 1) are as follows:

Format 2 : Format 1 with block number added.

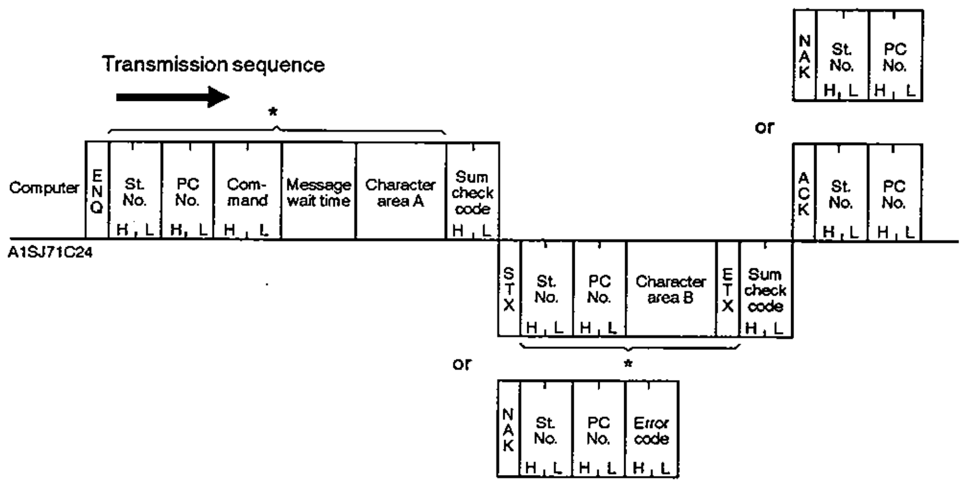
Format 3 : Format 1 with STX and ETX added.

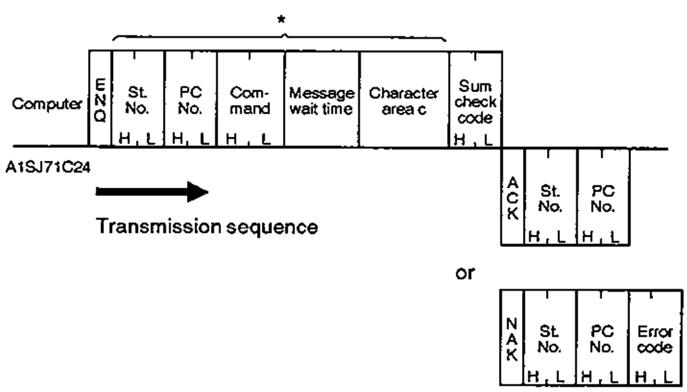
Format 4 : Format 1 with CR and LF added.

The following sections describe details of the four control protocols and the meanings of individual items.

8.4.1 Control format 1

St. No. : Station number

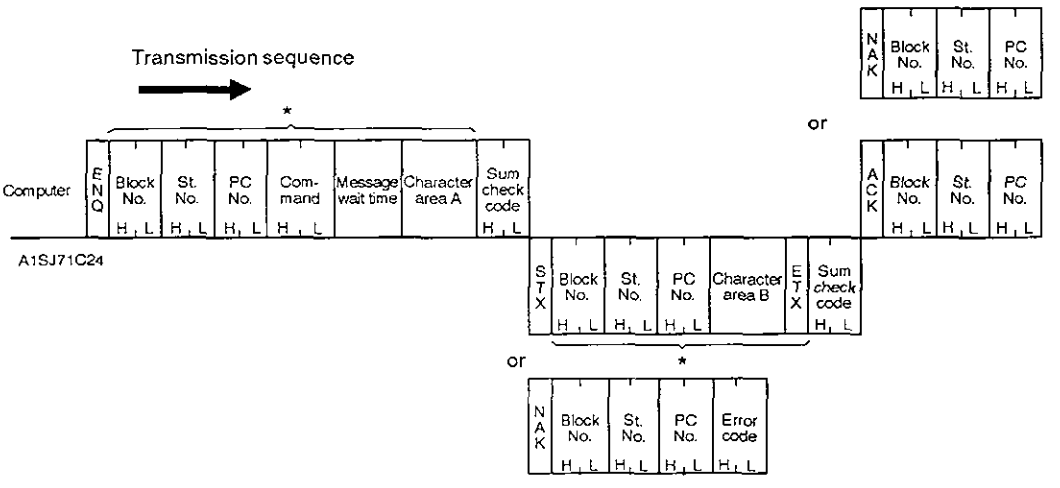
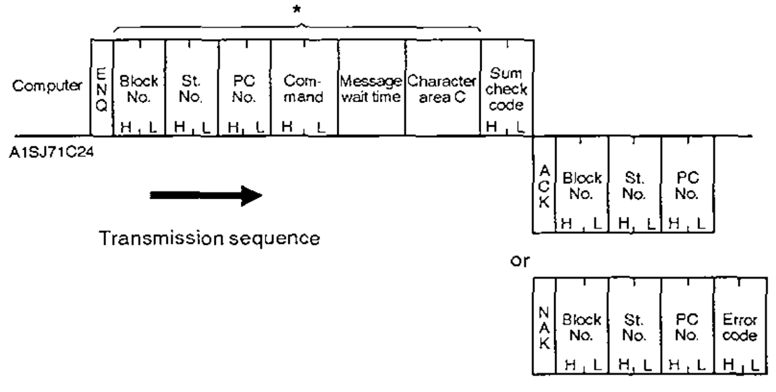
<table>
<tr><th>Description</th><th>Control Protocol</th></tr>
<tr><td>To read data from the PC CPU to the computer</td><td>


</td></tr>
<tr><td>To write data from the computer to the PC CPU</td><td>


</td></tr>
<tr><td>Remarks</td><td>(1) The sum check is enabled by DIP switch 12.
The sum check code only exists when the sum check is enabled by turning DIP switch 12 ON.
(2) The sum check is made for characters marked "*" in these diagrams.
(3) In these diagrams, the contents of "character area A", "character area B", and "character area C" depend on the individual system. For details, see the relevant sections. The contents of all character areas are the same for all 4 formats.</td></tr>
</table>

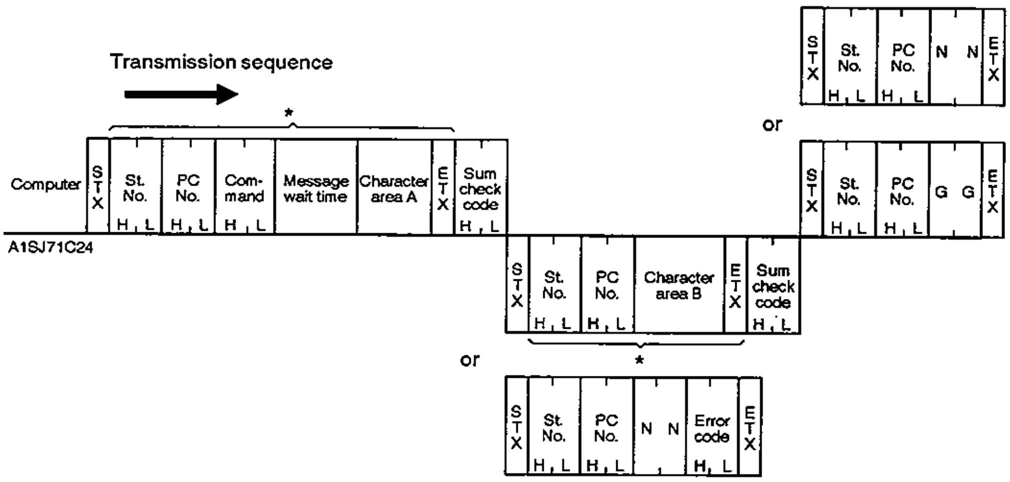
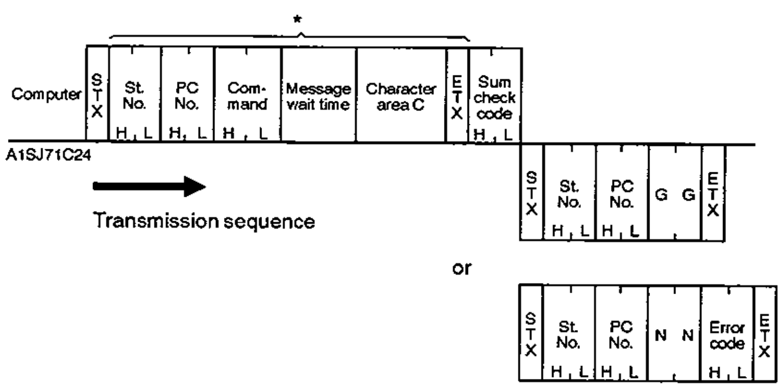
8.4.2 Control format 2

St. No. : Station number

<table>
<tr><th>Description</th><th>Control Protocol</th></tr>
<tr><td>To read data from the PC CPU to the computer</td><td>
</td></tr>
<tr><td>To write data from the computer to the PC CPU</td><td>
</td></tr>
<tr><td>Remarks</td><td>(1) The sum check is enabled by DIP switch12.
The sum check code only exists when the sum check is enabled by turning DIP switch 12 ON.
(2) The sum check is made for characters marked "*" in these diagrams.
(3) In these diagrams, the contents of "character area A", "character area B", and "character area C" depend on the individual system. For details, see the relevant sections. The contents of all character areas are the same for all 4 formats.</td></tr>
</table>

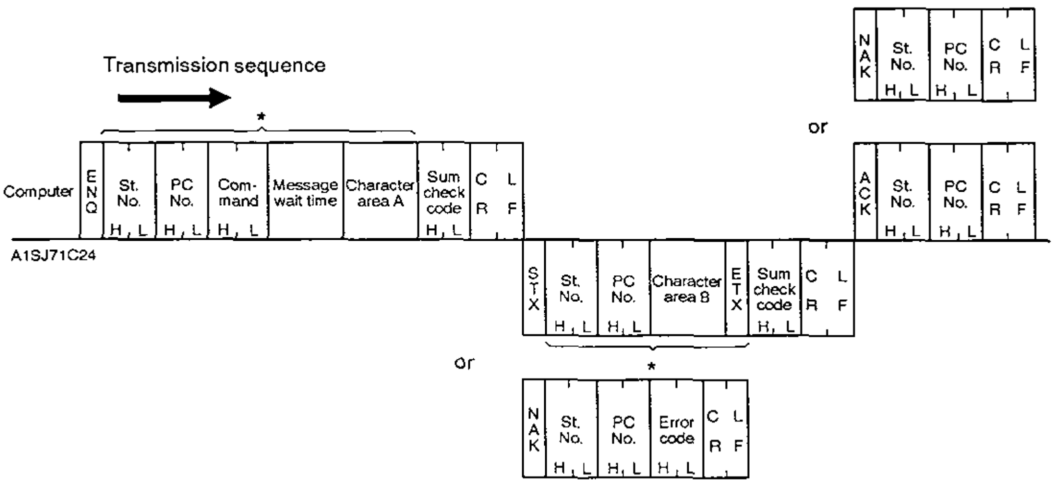
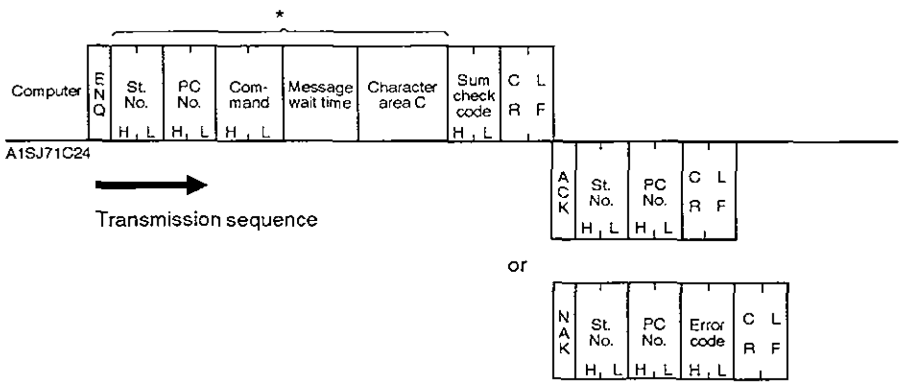
8.4.3 Control format 3

St. No. : Station number

<table>
<tr><th>Description</th><th>Control Protocol</th></tr>
<tr><td>To read data from the PC CPU to the computer</td><td>
</td></tr>
<tr><td>To write data from the computer to the PC CPU</td><td>
</td></tr>
<tr><td>Remarks</td><td>(1) The sum check is enabled by DIP switch 12.
The sum check code only exists when the sum check is enabled by turning DIP switch 12 ON.
(2) The sum check is made for characters marked "*" in these diagrams.
(3) In these diagrams, the contents of "character area A", "character area B", and "character area C" depend on the individual system. For details, see the relevant sections. The contents of all character areas are the same for all 4 formats.</td></tr>
</table>

8.4.4 Control format 4

St. No. : Station number

<table>
<tr><th>Description</th><th>Control Protocol</th></tr>
<tr><td>To read data from the PC CPU to the computer</td><td>
</td></tr>
<tr><td>To write data from the computer to the PC CPU</td><td>
</td></tr>
<tr><td>Remarks</td><td>(1) The sum check is enabled by DIP switch 12.
The sum check code only exists when the sum check is enabled by turning DIP switch 12 ON.
(2) The sum check is made for characters marked "*" in these diagrams.
(3) In these diagrams, the contents of "character area A", "character area B", and "character area C" depend on the individual system. For details, see the relevant sections. The contents of all character areas are the same for all 4 formats.</td></tr>
</table>

8.4.5 Setting protocol data

(1) Control code

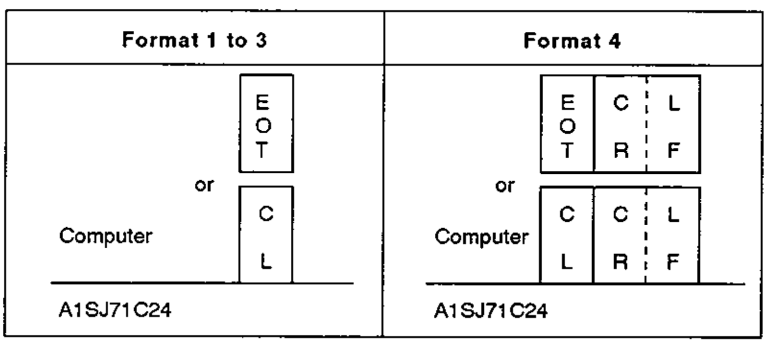
All control codes are sent and received in hexadecimal. They are shown in the following table.

Signal	Code (Hexadecimal)	Description	Signal	Code (Hexadecimal)	Description
NUL	00H	Null	LF	0AH	Line Feed
STX	02H	Start of Text	CL	0CH	Clear
ETX	03H	End of Text	CR	0DH	Carriage Return
EOT	04H	End of Transmission	NAK	15H	Negative Acknowledge
ENQ	05H	Enquiry	G	47H	Good
ACK	06H	Acknowledge	N	4EH	No Good

(a) The NUL code (00H) is ignored in all messages. If a NUL code is included in a message, it is processed as if it did not exist.

(b) In format 3, control code "GG" is equivalent to ACK and "NN" is equivalent to NAK.

(c) After receiving an EOT or CL code, the A1SJ71C24 initializes transmission but does not answer. The initializing code depends on the format as indicated below. At this time there is no answer from the A1SJ71C24.



(2) Block number

The block number is an optional number assigned as a data reference number for the computer. Block numbers are used to arrange data, etc. Block numbers may be from 00H to FFH in 2-digit ASCII (hexadecimal).

(3) Station number

The A1SJ71C24 is not equipped with a station number setting switch. Allot station number 00H to an A1SJ71C24.

(4) PC CPU number

The PC CPU number determines which PC CPU on MELSECNET/B to access.

The PC CPU number may be from 00H to 40H (00H to 1FH in MELSEC-NET/B) in 2-digit ASCII (hexadecimal).

(a) Accessing PC CPUs of other stations in a MELSECNET(/B) of an A1SCPU

Set all PC CPU numbers to FFH (self) using the computer. Use any function except the on-demand function.

(b) Accessing PC CPUs on MELSECNET(/B) equipped with A1SJ71C24

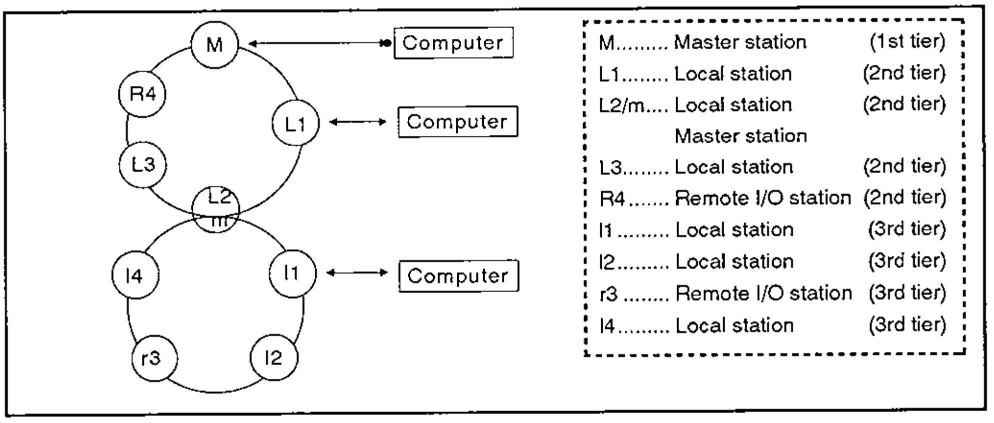
1) When computer and master station are connecterd

- MELSECNET local and remote I/O stations: Set each slave link station number (1 to 64) in hexadecimal (01H to 40H)
- MELSECNET/B local stations: Set each slave link station number (1 to 32) in hexadecimal (01H to 1FH).

2) When computer and A1SJ71C24-R2 of a local station are connected
MELSECNET/B master stations: Set the PC CPU number to 00H

(c) The range of PC CPUs which can be accessed by setting the PC CPU numbers is shown below.

1) MELSECNET



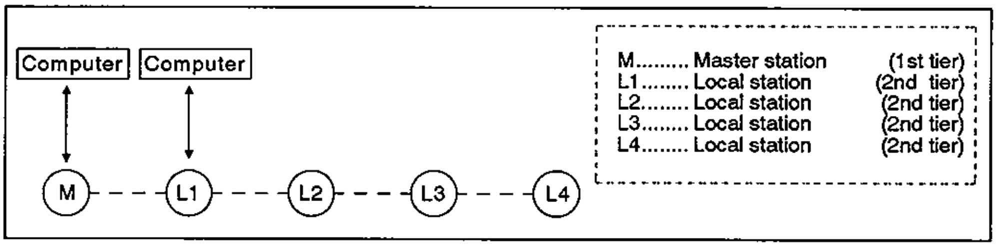
A1SCPU Loaded with A1SJ71C24 Connected to Computer	PC CPUs to Which a Link is Possible (PC CPU Number)									
	Self (FF)	M (0)	L1 (1)	L2/m (2/0)	L3 (3)	R4 (4)	l1 (1)	l2 (2)	r3 (3)	l4 (4)
M	o	–	o	o	o	o *1	x	x	x	x
L1	o	o	–	x	x	x	x	x	x	x
l1	o	x	x	o	x	x	–	x	x	x

o...... Access to all devices possible by setting appropriate PC CPU numbers
o*1.... Access to special-function module buffer memory possible by setting appropriate PC CPU numbers

POINT

Communications is not possible with A0J2CPUP23/R25 or A0J2CPUP25/R25 CPUs.

2) MELSECNET/B

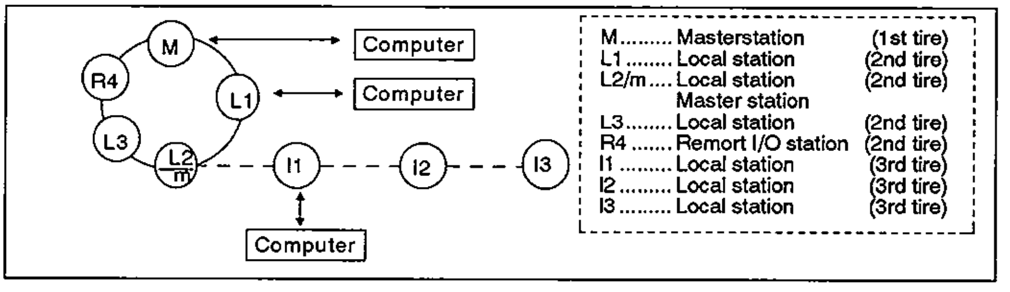


A1SCPU Loaded with A1SJ71C24 Connected to Computer	PC CPUs to Which a Link is Possible (PC CPU Number)					
	Self (FF)	M (0)	L1 (1)	L2 (2)	L3 (3)	L4 (4)
M	o	–	o	o	o	o
L1	o	o	–	x	x	x

o...... Access to all devices possible by setting appropriate PC CPU numbers

3) Mult mode of MELSECNET and MELSECNET/B

- MELSECNET is used for the 1st 2nd tiers, and MELSECNET/B is used for the 3rd tier



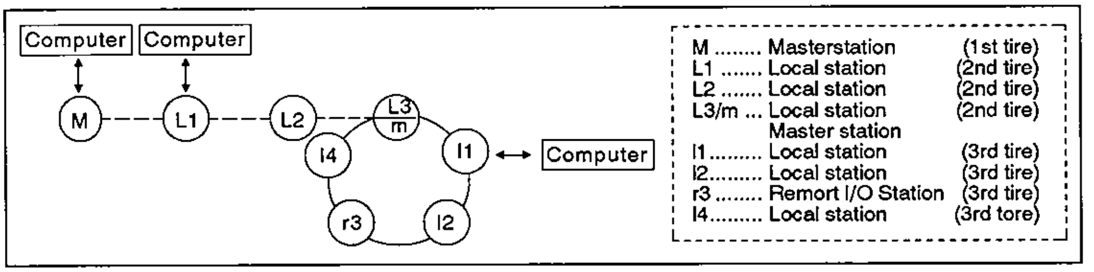
A1SCPU Loaded with A1SJ71C24 Connected to Computer	PC CPUs to Which a Link is Possible (PC CPU Number)								
	Self (FF)	M (0)	L1 (1)	L2/m (2/0)	L3 (3)	R4 (4)	I1 (1)	I2 (2)	I3 (3)
M	o	–	o	o	o	o *1	x	x	x
L1	o	o	–	x	x	x	x	x	x
I1	o	x	x	o	x	x	–	x	x

o...... Access to all devices possible by setting appropriate PC CPU numbers
o*1.... Access to special-function module buffer memory possible by setting appropriate PC CPU numbers

POINT

Communications with an A0J2CPUP23/R23 or an A0J2P25/R25 is not possible.

- MESLECNET is used for the 1st and the 2nd tires, and MELSECNET/B is used for the 3rd tire



A1SCPU Loaded with A1SJ71C24 Connected to Computer	PC CPUs to Which a Link is Possible (PC CPU Number)								
	Self (FF)	M (0)	L1 (1)	L2 (2)	L3/m (3/0)	R4 (4)	I1 (1)	r3 (3)	14 (4)
M	o	–	o	o	o	x	x	x	x
L1	o	o	–	x	x	x	x	x	x
I1	o	x	x	o	x	x	–	x	x

o...... Access to all devices possible by setting appropriate PC CPU numbers

(5) Command

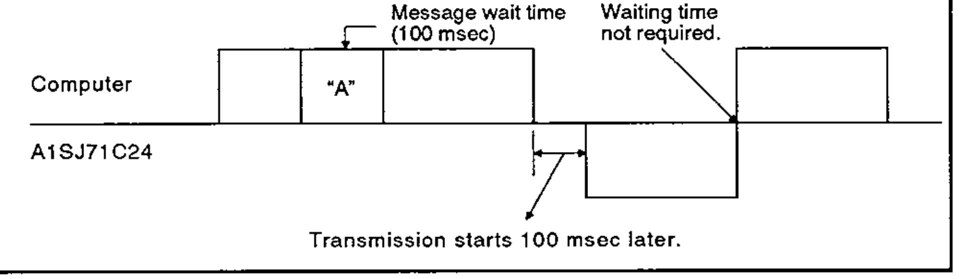
Used to specify the operation required, e.g. read, write, etc. Commands must be in 2-digit ASCII.

(6) Message wait time

This is a time delay required for some computers to switch from send to receive states. The message wait time determines the minimum waiting time before the A1SJ71C24 sends data after receiving it from the computer. Set this time in accordance with the computer specifications.

The message wait time may be set between 0 and 150 msec in units of 10 msec. The time is set from 0H to FH (0 to 15) in 1-digit hexadecimal, where 1 corresponds to 10 msec,

Example: Setting the message wait time

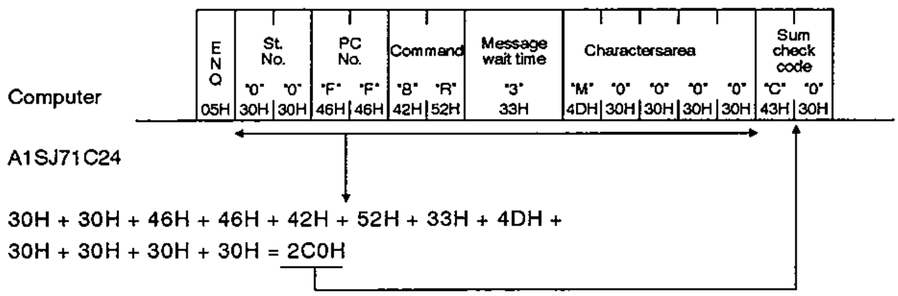


(7) Sum check code

The sum check code is 2-digit ASCII representing the lower 1 byte (8 bits) of the sum derived from the BIN code representing the checked data.

With DIP switch SW12 OFF, the sum check code is not added.

Example: If M,0,0,0 and 0 are transferred in format 1, setting station number 0, PC CPU number FF, command BR (batch read of device memory), and message wait time to 30 msec, the sum check code value is as shown below



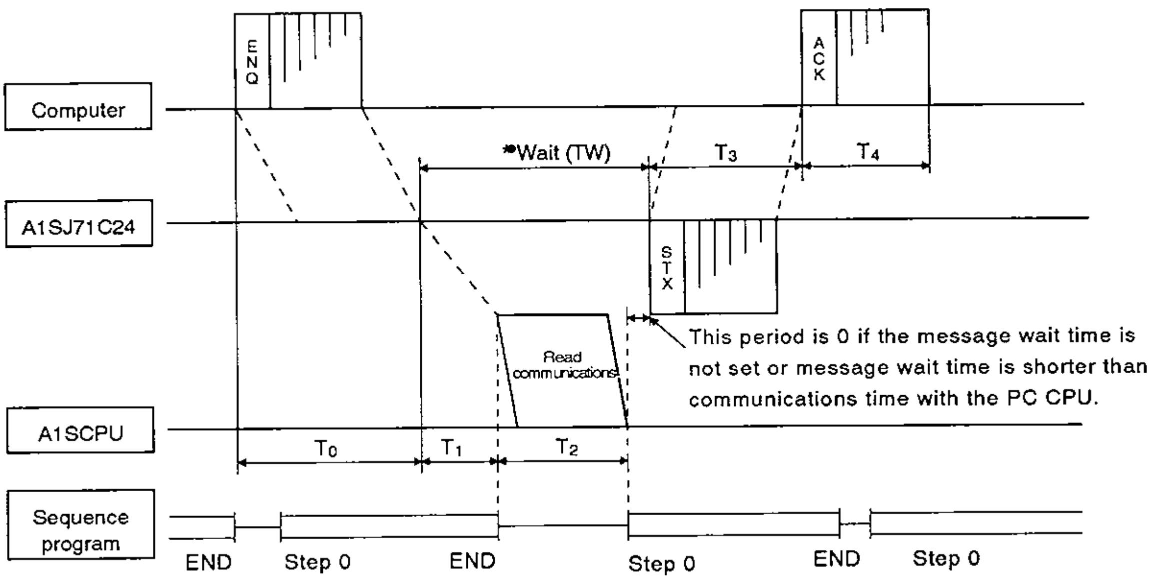
St. No. : Station number

(8) Error code

- Indicates an error following a NAK transmission.
- Error codes are transmitted as 2-digit ASCII (hexadecimal) in the range of 00H to FFH.
- If two or more errors occur simultaneously, the error code of the lowest number is transmitted.
- For error code details, see Section 11.1.

8.5 Transmission Sequence Timing Charts and Communications Time

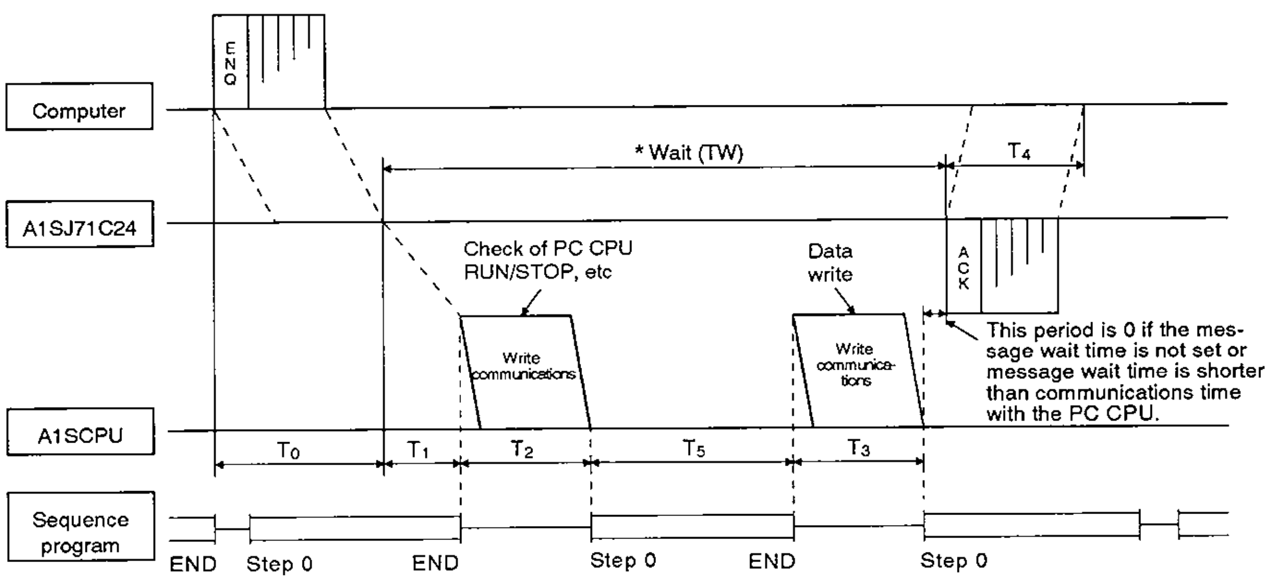
(1) To read data from the A1SCPU to the computer
("*" indicates that the message wait time has been set.)



REMARK

For file register and parameter, an extra 1 scan plus T2 is required.

(2) To write data from the computer to the A1SCPU
("*" indicates that message wait time has been set.)



REMARKS

As shown above, communications between the A1SJ71C24 and the A1SCPU is always made after END. Therefore, the scan time is extended by the time used for communications.

Appendix 5 gives the communications time.

Section 3.3.1 gives the number of points processed per communication after END.

(3) Communications time

This section describes how to calculate approximate communications time from the start of data transmission from the computer to the completion of all communications after a reply is sent from the A1SJ71C24.

For T0 to T4, see (1) and (2) on the previous page.

(a) To read data from the A1SCPU to the computer

Communications time = T0 + (longer time of T1 + T2 or TW) + T3 + T4

where,

T0, T3, T4 = 1/baud rate X the number of bits per character

$$(\underbrace{1}_{\text{Start bit}} + \underbrace{7/8}_{\text{Data length (7 or 8)}} + \underbrace{0/1}_{\text{Parity bit (0 or 1)}} + \underbrace{1/2}_{\text{Stop bit (1 or 2)}}) \times \text{the character length}$$

T1 = maximum 1 scan time (since data entry to the PC CPU is made after END processing. If the PC CPU is not running, T1 is 0.)

T2 = value in Appendix 5

TW = message wait time

(b) To write data from the computer to the A1SCPU

Communications time =
T0 + (longer time of T1 + T2+ T3 + T5 or TW) + T4

where,

T0, T4 = 1/baud rate X the number of bits per character

$$(\underbrace{1}_{\text{Start bit}} + \underbrace{7/8}_{\text{Data length (7 or 8)}} + \underbrace{0/1}_{\text{Parity bit (0 or 1)}} + \underbrace{1/2}_{\text{Stop bit (1 or 2)}}) \times \text{the character length}$$

T1 = maximum 1 scan time (since data entry to the PC CPU is made after END processing. If the PC CPU is not running, T1 is 0.)

T2, T3 = value in Appendix 5
(For functions processed in 1 scan, T3 is 0.)

TW = message wait time

T5 = 1 scan time
(For functions processed in one scan, T5 is 0.)

(4) Transmission time through MELSECNET/B

(a) The transmission time (T1) for data transmission by specifying the PC CPU number to a PC CPU on MELSECNET/B not equipped with an A1SJ71C24 is calculated as follows:

- Local station

  Transmission time (T1) = (LRDP instruction processing time + scan time for station 1 loaded with A1SJ71C24) x 2

- Causes of delayed transmission time (T1)

  Instructions requiring 2 scans for transmission (writing to device "R", etc.) need double the time derived from the equations above.

  When other stations in the link are being monitored by an A6GPP, the transmission time doubles for each station to be monitored.

  The Data Link Reference Manual gives details of the data link.

Example:

The transmission time for a MELSECNET/B master station equipped with A1SJ71C24 to read a local station device memory:

(Conditions: L<LS<M, M : 80 msec $\alpha1$: 10 msec)

$$\text{Transmission time T1} = (M \times 4 + \alpha1 \times 4 + M) \times 2$$
$$= (80 \times 4 + 10 \times 4 + 80) \times 2 = 880$$

The transmission time is 880 msec. Where:

M : MELSECNET/B master station scan time

$\alpha1$: MELSECNET/B master station link refresh time

LS : Link scan time

L : MELSECNET/B local station scan time

POINT

Under some conditions, data transmission to a PC CPU on MELSECNET/B not equipped with an A1SJ71C24 can cause a considerable time delay.

This time delay can be reduced by carrying out all communications from the computer to PC CPUs to stations equipped with an A1SJ71C24 (PC CPU station number FFH) and all other data communications using the MELSECNET/B data link (B, W).

8.6 Character Area Data Transmission

The concept of transmission data handled as character areas when using commands to carry out data communications between the computer and the A1SCPU is explained in this section. The data shown in the examples is contained in character area B in the case of read and monitor, and in character area C in the case of write, test, and monitor data register.

(1) Bit device memory read and write

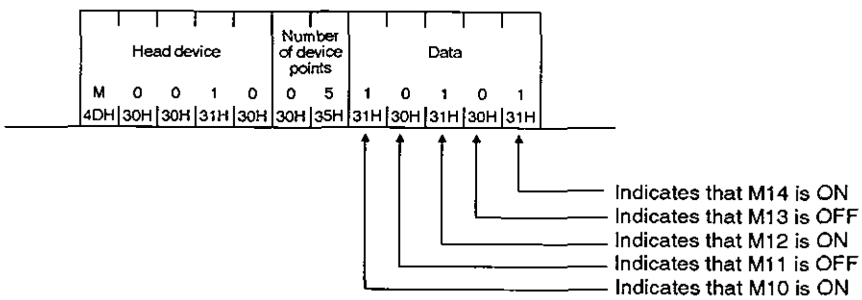
The bit device memory can be handled in bit units (1 device point) or word units (16 device points).

These units are described below.

(a) Bit units (1 point)

When the bit device memory is handled as bit units, the specified number of device points from the specified head device in sequence from the left are represented as 1 (31H) if the device is ON, or 0 (30H) if the device is OFF.

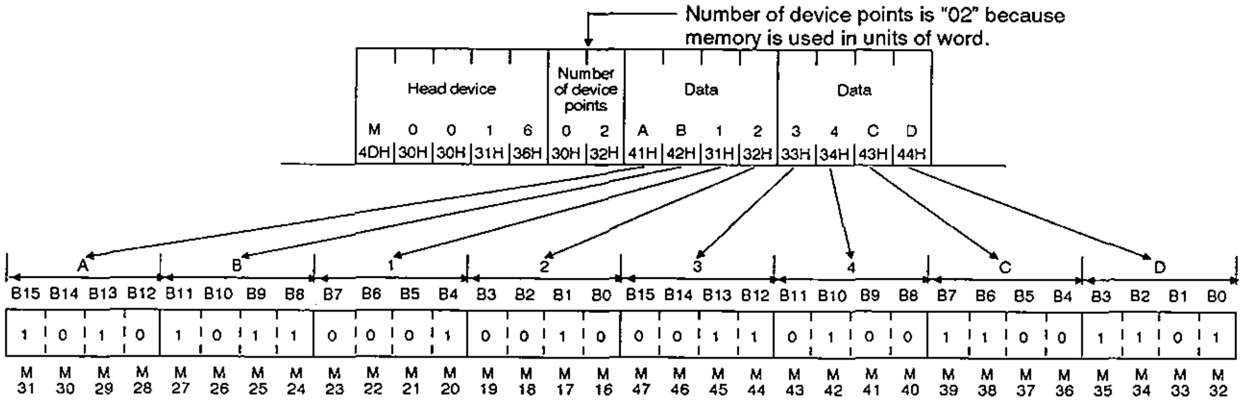
Example: Indication of the ON/OFF status of 5 points from M10



(b) Word units (16 points)

When the bit device memory is handled as word units, each word is expressed sequentially in hexadecimal values in 4-bit units from the higher bit.

Example: Indication of the ON/OFF status of 32 points from M16



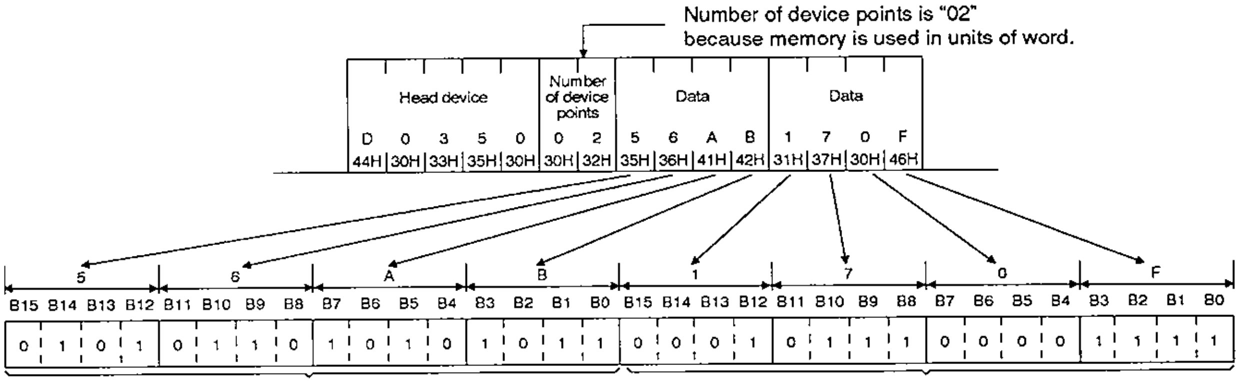
0 : represents ON

1 : represents OFF

(2) Word device memory read and write

In the word device memory, each word is expressed sequentially in hexadecimal values in 4-bit units from the higher bit.

Example: Indication of the contents of the D350 and D351 registers



Indicates that the content of register D350 is 56ABH (22187 in decimal)

Indicates that the content of register D351 is 170FH (5903 in decimal)

REMARKS

(1) Extension file memory read and write, buffer memory read and write, and on-demand data when word units are specified are handled according to the same principle as the word device memory.

(2) To output a character-string with the PR instruction externally after transmitting it from the computer to the A1SCPU, the processing should be as shown below:

1) The character-string to be transmitted is developed into 2-byte codes in units of characters.

Example: To transmit "18AFH $^{C}{}_{R}$" to a sequence program.

	"1"	"8"	"A"	"F"	"H"	"$^{C}{}_{R}$"
Codes.....	31H	38H	41H	46H	48H	0DH
	33H 31H	33H 38H	34H 31H	34H 36H	34H 38H	30H 44H
	"3" "1"	"3" "8"	"4" "1"	"4" "6"	"4" "8"	"0" "D"

2) The character-string developed into 2-byte codes is arranged in units of 2 characters and sent to the A1SJ71C24.

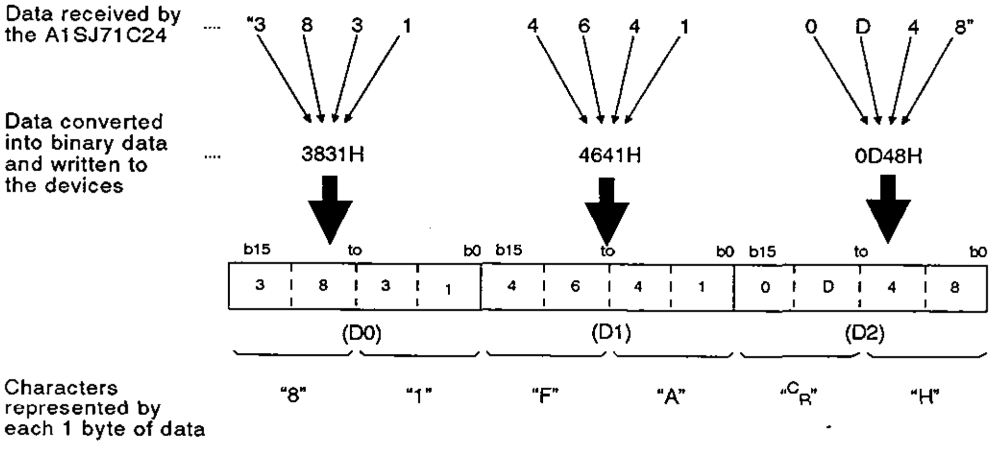
Example: The character-string used in the above example in 1.

"31 38 41 46 48 0D" "383146410D48"

"383146410D48" is sent from the computer to the A1SJ71C24.

The A1SJ71C24 converts the data sent from the computer into binary data and writes it to the designated device.

Example: To write the data composed in the above example in 2) to D0 to D2 in the A1SCPU.



8.7 Device Memory Read/Write

8.7.1 Commands and device ranges

(1) The ACPU common commands and device ranges used for device memory read/write are described below.

(a) ACPU common commands

Item		Command: Symbol	Command: ASCII Code	Processing Contents	Number of Points Processed per Communi-cations	PC CPU Status: During STOP	PC CPU Status: During RUN SW04 ON	PC CPU Status: During RUN SW04 OFF	Access to A1SCPU	Access to PC CPU in Data Link
Batch Read	Bit units	BR	42H, 52H	Reads bit devices (X, Y, M, etc.) in units of points.	256 points	o	o	o	o	o
	Word units	WR	57H, 52H	Reads bit devices (X, Y, M, etc.) in units of 16 points.	32 words (512 points)				o	o
				Reads word devices (D, R, T, C, etc.) in units of points.	64 points					
Batch Write	Bit units	BW	42H, 57H	Writes data to bit devices (X, Y, M, etc.) in units of points.	160 points	o	o	x	o	o
	Word units	WW	57H, 57H	Writes data to bit devices (X, Y, M, etc.) in units of 16 points.	10 words (160 points)					
				Writes data to word devices (D, R, T, C, etc.) in units of points.	64 points					
Test (Random Write)	Bit units	BT	42H, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of points by designating the devices and device numbers at random.	20 points	o	o	x	o	o
	Word units	WT	57H, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of 16 points by designating the devices and device numbers at ran-dom.	10 words (160 points)				o	o
				Writes data to word devices (D, R, T, C, etc.) in units of points by designating the devices and device numbers at random.	10 points					
Monitor Data Regis-tration	Bit units	BM	42H, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of points.	40 points*	o	o	o	o	o
	Word units	WM	57H, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of 16 points.	20 words* (320 points)				o	o
				Sets the word devices (D, R, T, C, etc.) to be monitored in units of points.	20 points					
Monitor	Bit units	MB	4DH, 42H	Monitors the devices registered formonitoring.	—	o	o	o	o	o
	Word units	MN	4DH, 4EH							

Note : o........Executable
x.........Not executable

For the number of processing points indicated by an asterisk (*), the number is one half of the values indicated in the table for the input device (x) when PC CPUs other than the A3H CPU, A2ACPU(S1), and A3ACPU are used. (See *1 in 3.3.1 (1).)

POINT

When a MELSECNET or MELSECNET/B data link system is used, the PC CPUs of other stations are also accessible.
When ACPU common commands are used to access the devices in an A2ACPU(S1) or A3ACPU of other station, the device number ranges described in (b) can be used.

Use the AnACPU dedicated commands described in (2) to access the extension devices.

(b) Device ranges when ACPU common commands are used

The devices and device number ranges that can be used for the device memory access operation are described below.

The device designation code consists of 5 characters.

Leading zeros in the device number (underlined zeros in X0070, for example) can be expressed with a blank code (20H).

Device	+	Device number	=5 characters
1 character (2 characters for T/C)		4 characters (3 characters for T/C)	

Bit Device			Word Device		
Device	Device Number Ranges (Characters)	Decimal/ Hexadecimal Expression	Device	Device Number Range (Characters)	Decimal/ Hexadecimal Expression
Input X	X0000 to X07FF	Hexadecimal	Timer (present value) T	TN000 to TN255	Decimal
Output Y	Y0000 to Y07FF	Hexadecimal	Counter (present value) C	CN000 to CN255	Decimal
Internal relay M	M0000 to M2047	Decimal	Data register D	D0000 to D1023	Hexadecimal
Latch relay L	L0000 to L2047	Decimal	Link register W	W0000 to W03FF	Hexadecimal
Step relay S	S0000 to S2047	Decimal	File register R	R0000 to R8191	Hexadecimal
Link relay B	B0000 to B03FF	Hexadecimal	Special register D	D9000 to D9255	Decimal
Annunciator F	F0000 to F0255	Decimal			
Special relay M	M9000 to M9255				
Timer (contact) T	TS000 to TS255				
Timer (coil) T	TC000 to TC255				
Counter (contact) C	CS000 to CS255				
Counter (coil) C	CC000 to CC255				

POINTS

(1) To designate the bit device ranges in units of words, the bit device number must be a multiple of 16.

(2) Although the ranges are designated for M, L, and S, if the range for M is designated by L or S, the same processing occurs. This is also true for the ranges for L and S.

(3) The ranges of special relays (M9000 to M9255) and special registers (D9000 to D9255) are divided into the areas for read only, write only, and system use.

Trying to write data to the ranges outside the write-only area might cause the PC CPU to malfunction.

The ACPU programming manual gives details concerning special relays and special registers.

(4) When using the SW0GHP-UTLPC-FN1 utility software package or the dedicated instructions for the A2ACPU(S1) and A3ACPU extension file registers, use the commands explained in Section 8.8 for read and write operations for the file register (R).

(2) The AnACPU dedicated commands and device ranges used for device memory read/write are described below.

(a) AnACPU dedicated commands

Item		Command		Processing Contents	Number of Points Processed per Communications	PC CPU Status			Access to A1SCPU	Access to PC CPU in Data Link
		Symbol	ASCII Code			During STOP	During RUN SW04 ON	During RUN SW04 OFF		
Batch Read	Bit units	JR	4AH, 52H	Reads bit devices (X, Y, M, etc.) in units of points.	256 points	o	o	o	o	o
	Word units	QR	51H, 52H	Reads bit devices (X, Y, M, etc.) in units of 16 points.	32 words (512 points)				o	o
				Reads word devices (D, R, T, C, etc.) in units of points.	64 points					
Batch Write	Bit units	JW	4AH, 57H	Writes data to bit devices (X, Y, M, etc.) in units of points.	160 points	o	o	x	o	o
	Word units	QW	51H, 57H	Writes data to bit devices (X, Y, M, etc.) in units of 16 points.	10 words (160 points)				o	o
				Writes data to word devices (D, R, T, C, etc.) in units of points.	64 points					
Test (Random Write)	Bit units	JT	4AH, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of points by designating the devices and device numbers at random.	20 points	o	o	x	o	o
	Word units	QT	51H, 54H	Sets/resets bit devices (X, Y, M, etc.) in units of 16 points by designating the devices and device numbers at random.	10 words (160 points)				o	o
				Writes data to word devices (D, R, T, C, etc.) in units of points by designating the devices and device numbers at random.	10 points					
Monitor Data Registration	Bit units	JM	4AH, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of points.	40 points	o	o	o	o	o
	Word units	QM	51H, 4DH	Sets the bit devices (X, Y, M, etc.) to be monitored in units of 16 points.	20 words (320 points)				o	o
				Sets the word devices (D, R, T, C, etc.) to be monitored in units of points.	20 points					
Monitor	Bit units	MJ	4DH, 4AH	Monitors the devices registered for monitoring.	—	o	o	o	o	o
	Word units	MQ	4DH, 51H							

Note : o ....Executable

x.........Not executable

(b) Device ranges when AnACPU dedicated commands are used

The devices and device number ranges that can be used for device memory access operation are described below.

The device designation code consists of 7 characters.

Leading zeros in the device number (underlined zeros in X<u>000</u>070, for example) can be expressed with a blank code (20H).

Device	+	Device number	=7 characters
1 character (2 characters for T/C)		6 characters (5 characters for T/C)	

Bit Device			Word Device		
Device	**Device Number Range (Characters)**	**Decimal/ Hexadecimal Expression**	**Device**	**Device Number Range (Characters)**	**Decimal/ Hexadecimal Expression**
Input X	X000000 to X0007FF	Hexadecimal	Timer (present value) T	TN00000 to TN02047	Decimal
Output Y	Y000000 to Y0007FF	Hexadecimal	Counter (present value) C	CN00000 to CN01023	Decimal
Internal relay M	M000000 to M008191	Decimal	Data register D	D000000 to D006143	Hexadecimal
Latch relay L	L000000 to L008191	Decimal	Link register W	W000000 to W000FFF	Hexadecimal
Step relay S	S000000 to S008191	Hexadecimal	File register R	R000000 to R008191	Decimal
Link relay B	B000000 to B000FFF	Hexadecimal	Special register D	D009000 to D009255	Decimal
Annunciator F	F000000 to F002047	Decimal			
Special relay M	M009000 to M009255				
Timer (contact) T	TS00000 to TS02047				
Timer (coil) T	TC00000 to TC02047				
Counter (contact) C	CS00000 to CS01023				
Counter (coil) C	CC00000 to CC01023				

POINTS

(1) To designate the bit device ranges in units of words, the bit device number must be a multiple of 16.

For special relays M, whose device number is M9000 or greater, designation is possible by using "9000 + multiples of 16".

(2) Although the ranges are designated for M, L, and S, if the range for M is designated by L or S, the same processing occurs. This is also true for the ranges for L and S.

(3) The ranges of special relays (M9000 to M9255) and special registers (D9000 to D9255) are divided into the areas for read only, write only, and system use.

Trying to write data to the ranges outside the write-only area might cause the PC CPU to malfunction.

The ACPU programming manual gives details concerning special relays and special registers.

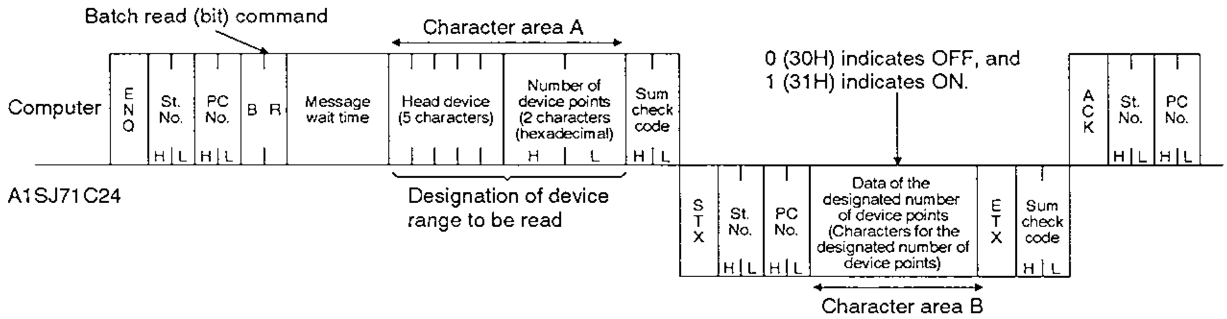
8.7.2 Batch read in units of bits

(a) Using the BR command (ACPU common commands)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



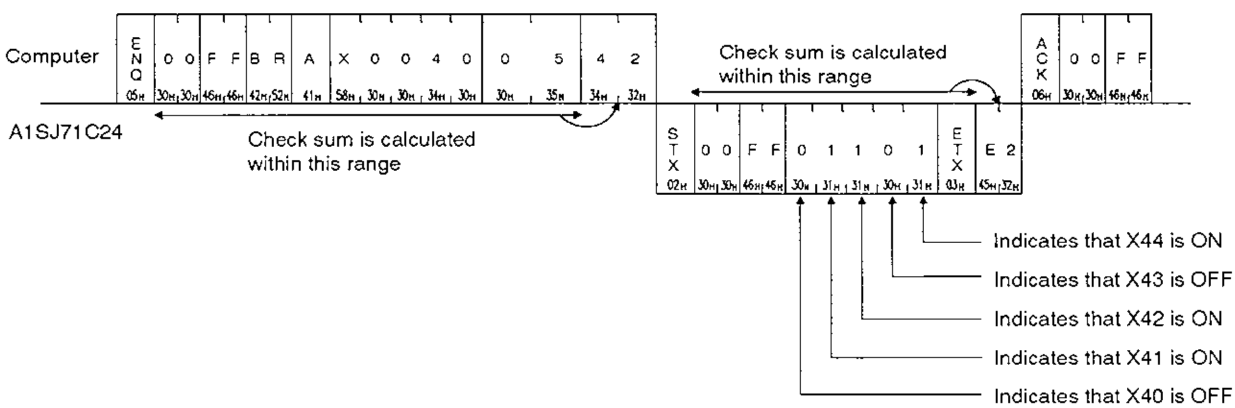
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 256 (setting for 256 points is 00H)
- (Head device number) + [(number of device points) − 1] ≤ maximum device number

Designation Example

To read the data at 5 points from X40 to X44 in A1SCPU. (Message wait time is 100 msec.) (Assume that X40 and X43 are OFF and X41, X42, and X44 are ON.)



POINT

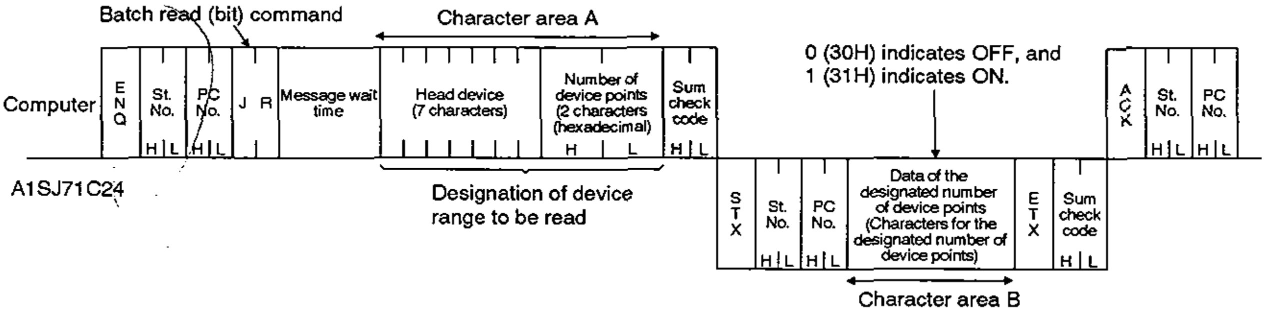
The message wait time is designated in the range of 0 to 150 msec in units of 10 msec, using hexadecimal notation of 0 through FH. Therefore, 100 msec corresponds to "A".

(b) Using the JR command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



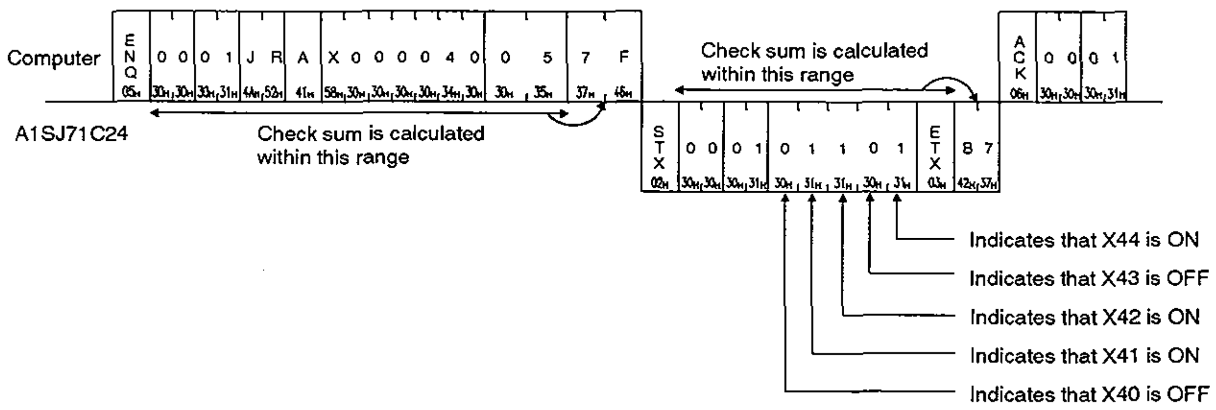
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 256 (setting for 256 points is 00H)
- (Head device number) + [(number of device points) − 1] ≤ maximum device number

Designation Example

To read the data at 5 points from X40 to X44 in PC NO. "01". (Message wait time is 100 msec.) (Assume that X40 and X43 are OFF and X41, X42, and X44 are ON.)



POINT

The message wait time is designated in the range of 0 to 150 msec in units of 10 msec, using hexadecimal notation of 0 to FH. Therefore, 100 msec corresponds to "A".

8.7.3 Batch read in units of words

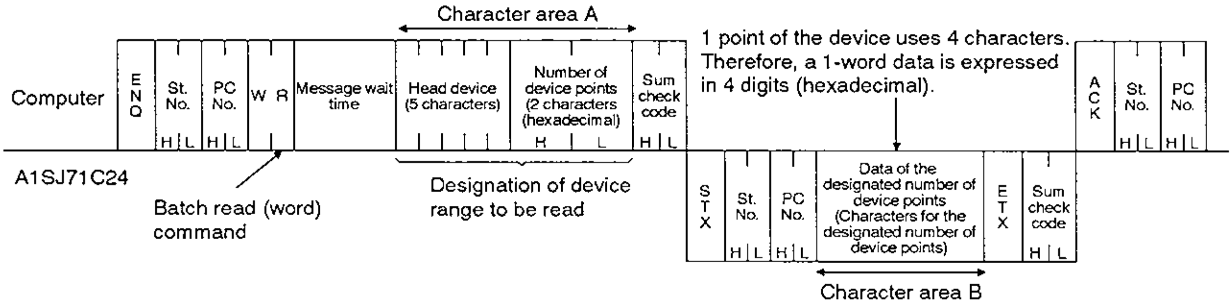
The method for specifying the control protocol and examples are shown below for a batch read of word device memory and batch read of bit device memory (16-point units).

(a) Using the WR command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



POINT

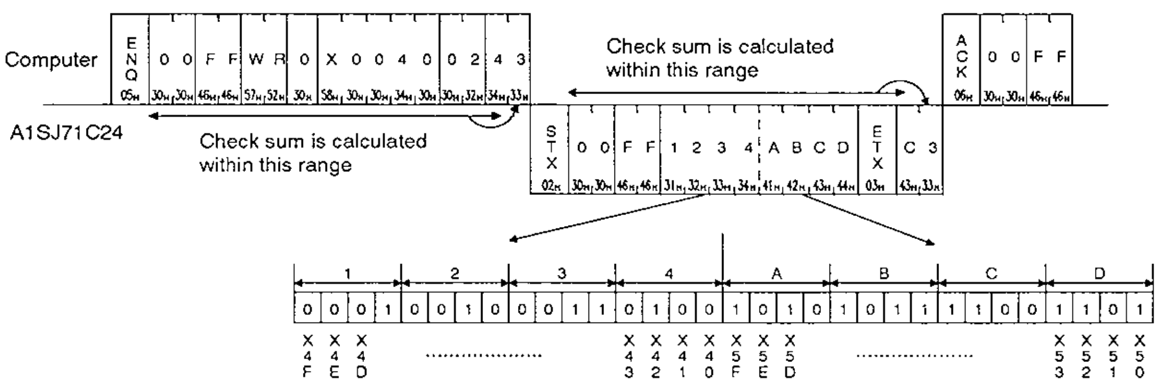
To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64 (32 for a bit device)
- (Head device number) + [(number of device points**) − 1] ≤ maximum device number

** ("number of device points" x 16 for a bit device)

Designation Examples

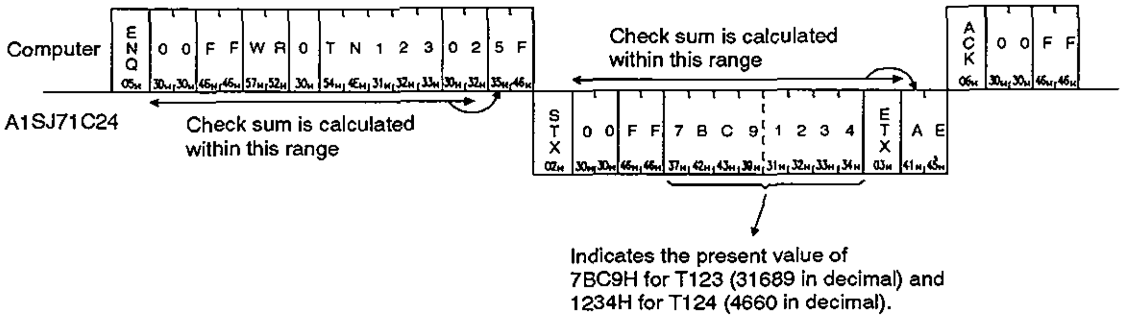
Example 1:
To read data at 32 points from X40 to X5F in A1SCPU.
(Message wait time is 0 msec)



POINT

The WR command is used for word unit designation. The designation for 32 points of devices from X40 to X5F is "02" ("1" for 16 points).

Example 2:
To read the present values at 2 points of T123 and T124 in A1SCPU.

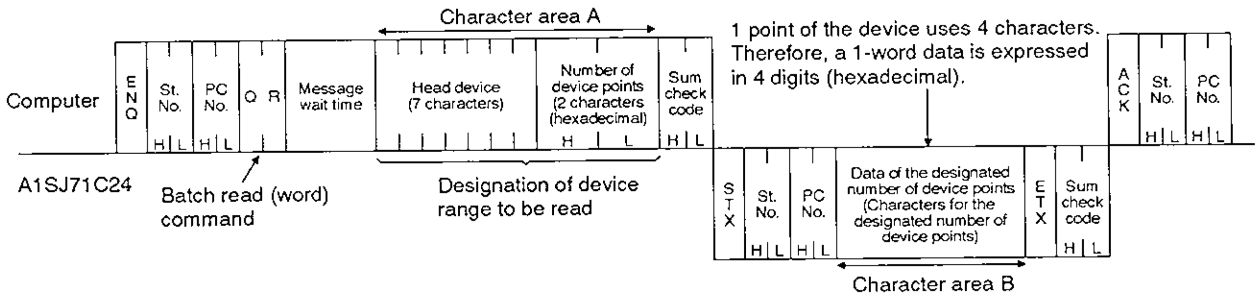


(b) Using the QR command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



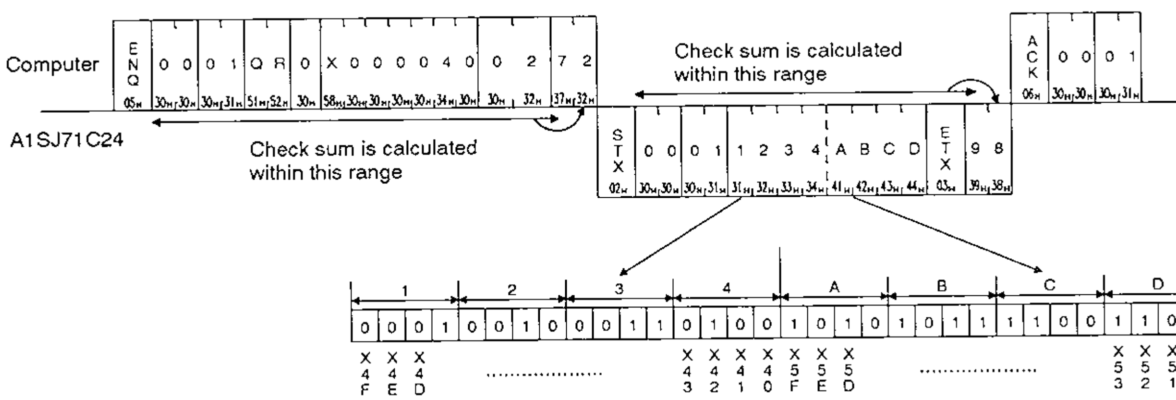
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64 (32 for a bit device)
- (Head device number) + [(number of device points**) − 1] ≤ maximum device number
  ** ("number of device points" x 16 for a bit device)

Designation Examples

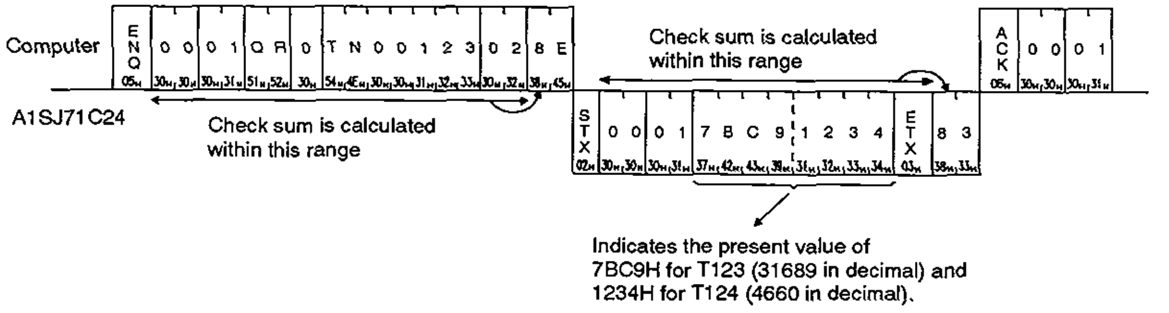
Example 1:
To read data at 32 points from X40 to X5F in PC NO. "01".
(Message wait time is 0 msec)



POINT

The QR command is used for word unit designation. The designation for 32 points of devices from X40 to X5F is "02" ("1" for 16 points).

Example 2:
To read the present values at 2 points of T123 and T124 in PC No. "01".



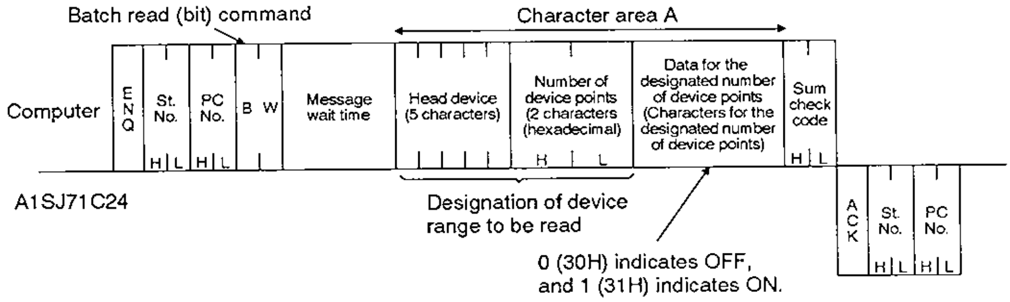
8.7.4 Batch write in units of bits

(a) Using the BW command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



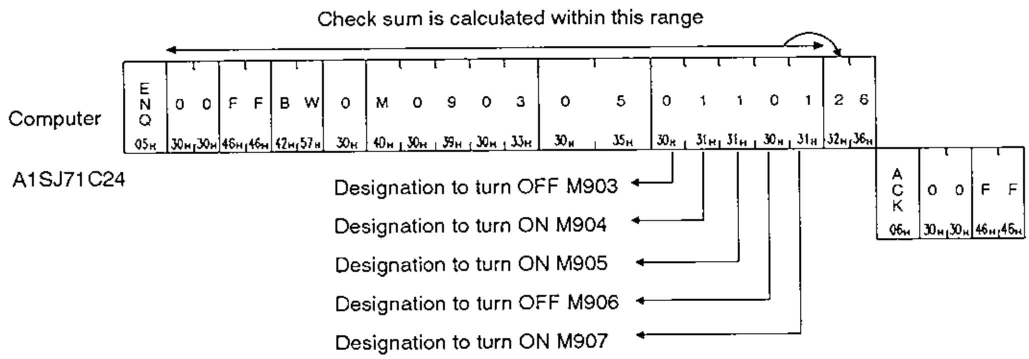
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 160
- (Head device number) + [(number of device points) − 1]≤ maximum device number

Designation Example

To write data to 5 points from M903 to M907 in A1SCPU.
(Message wait time is 0 msec)

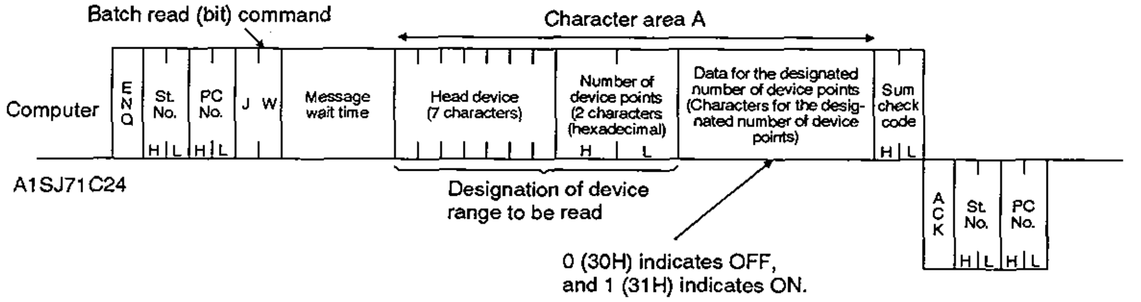


(b) Using the JW command (AnACPU common command)

Designation Method

Designation in protocol 1 is shown below.

St. No. : Station number



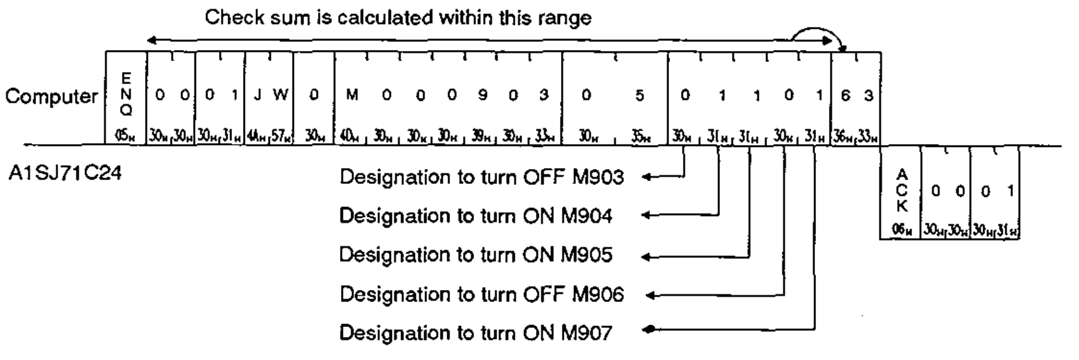
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 160
- (Head device number) + [(number of device points) − 1]≤ maximum device number

Designation Example

To write data to 5 points from M903 to M907 in PC NO. "0".
(Message wait time is 0 msec)



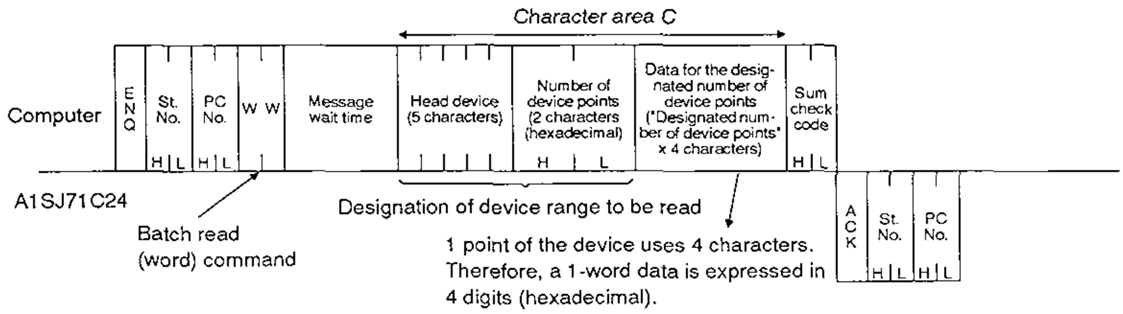
8.7.5 Batch write in units of words

(a) Using the WW command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



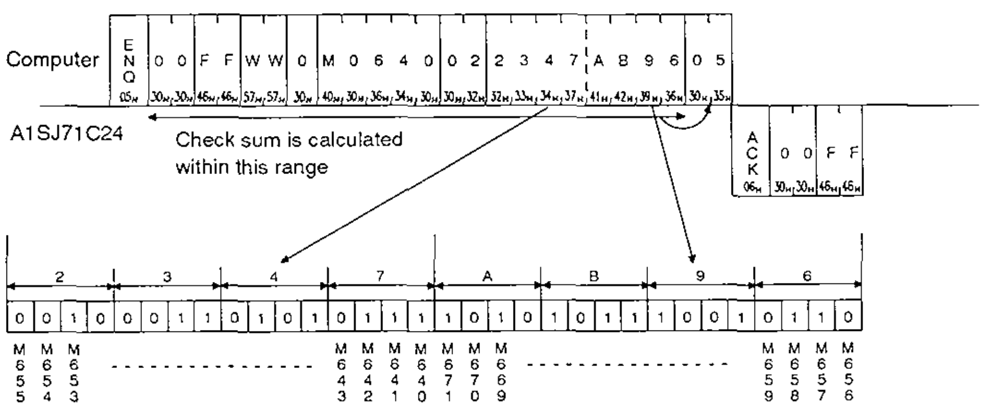
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64 (10 for a bit device)
- (Head device number) + [(number of device points**) − 1] ≤ maximum device number
  **("number of device points" x 16 for a bit device)

Designation Examples

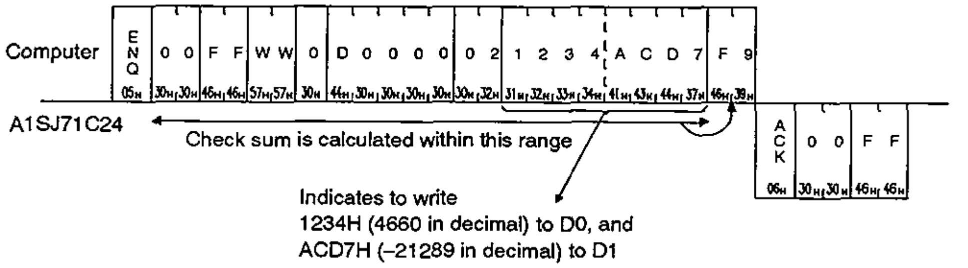
Example 1:
To write data to 32 points from M640 to M671 in A1SCPU.
(Message wait time is 0 msec)



POINT

The WW command is used for word unit designation. The designation for the number of device point to write data to the 32 points to M640 to M671 is "02" ("1" for 16 points).

Example 2: To write data to 2 points of D0 and D1 in A1SCPU.
(Message wait time: 0 mesc)

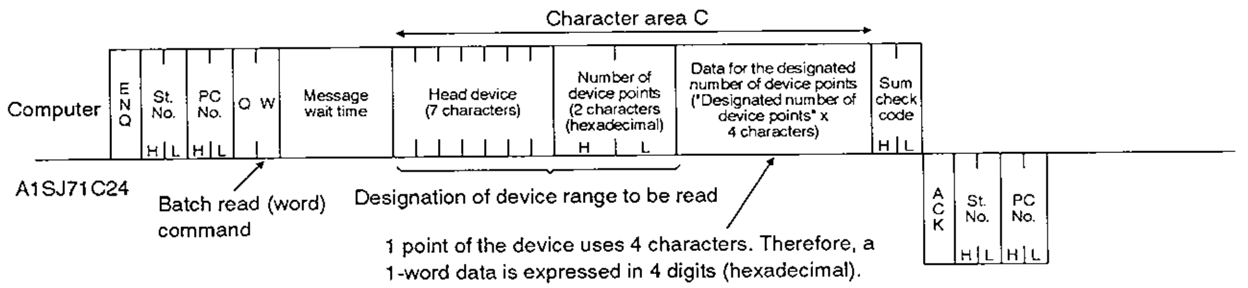


(b) Using the QW command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



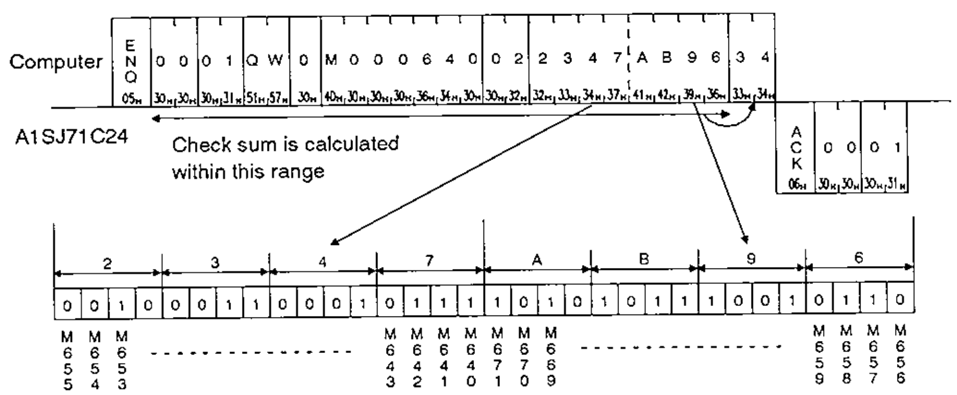
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64 (10 for a bit device)
- (Head device number) + [(number of device points**) − 1] ≤ maximum device number
  **("number of device points" x 16 for a bit device)

Designation Examples

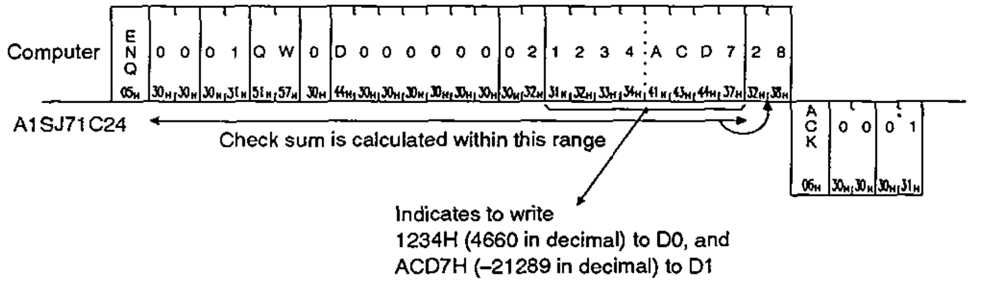
Example 1:
To write data to 32 points from M640 to M671 in A1SCPU.
(Message wait time is 0 msec)



POINT

The QW command is used for word unit designation. The designation for the number of device point to write data to 32 points from M640 to M671 is "02" ("1" for 16 points).

Example 2: To write data to 2 points of D0 and D1 in PC NO. "01".
(Message wait time: 0 mesc)



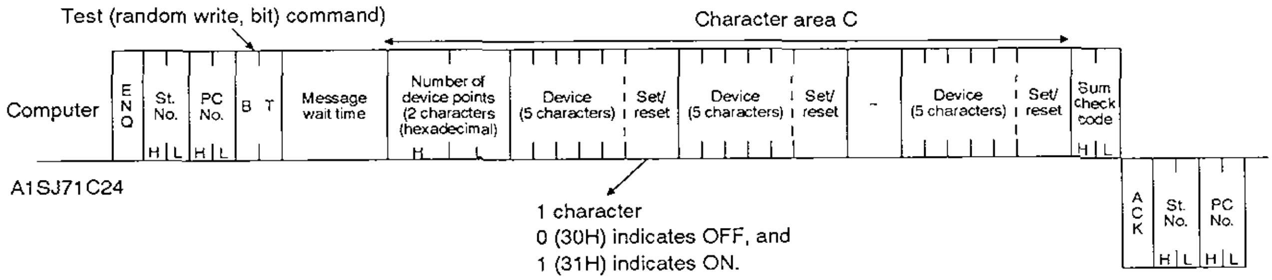
8.7.6 Testing device memory in units of bit (random write)

(a) Using the BT command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



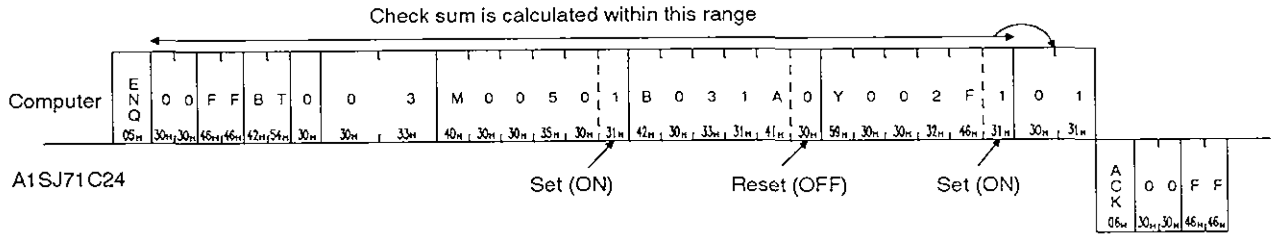
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 40

Designation Example

To write ON to M50, OFF to B31A, and ON to Y2F in A1SCPU.
(Message wait time is 0 msec)

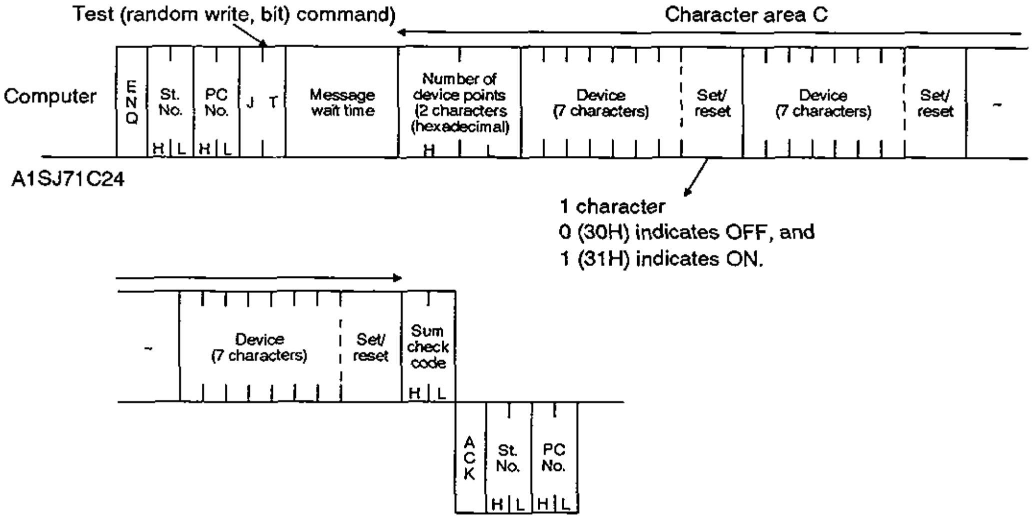


(b) Using the JT command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



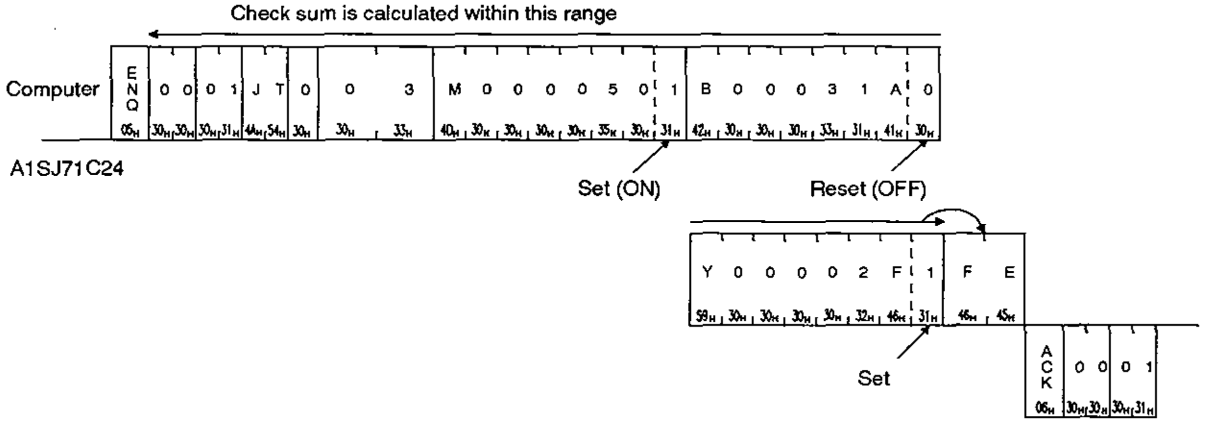
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 40

Designation Example

To write ON to M50, OFF to B31A, and ON to Y2F in PC NO. "01".
(Message wait time is 0 msec)



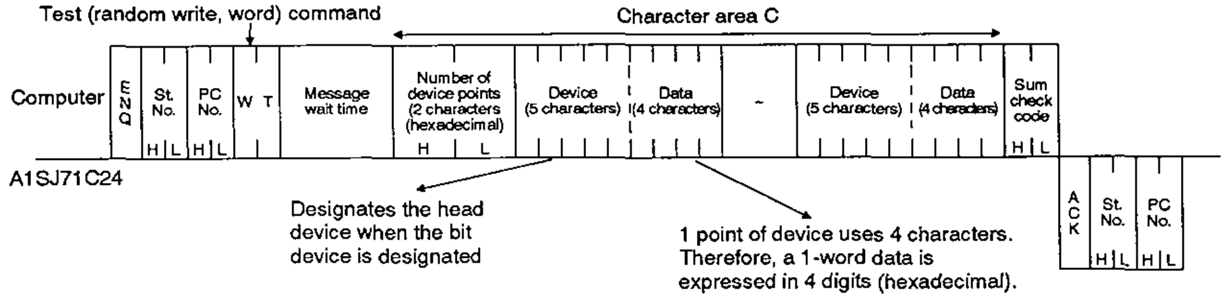
8.7.7 *Testing device memory in units of words (random write)*

(a) Using the WT command (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



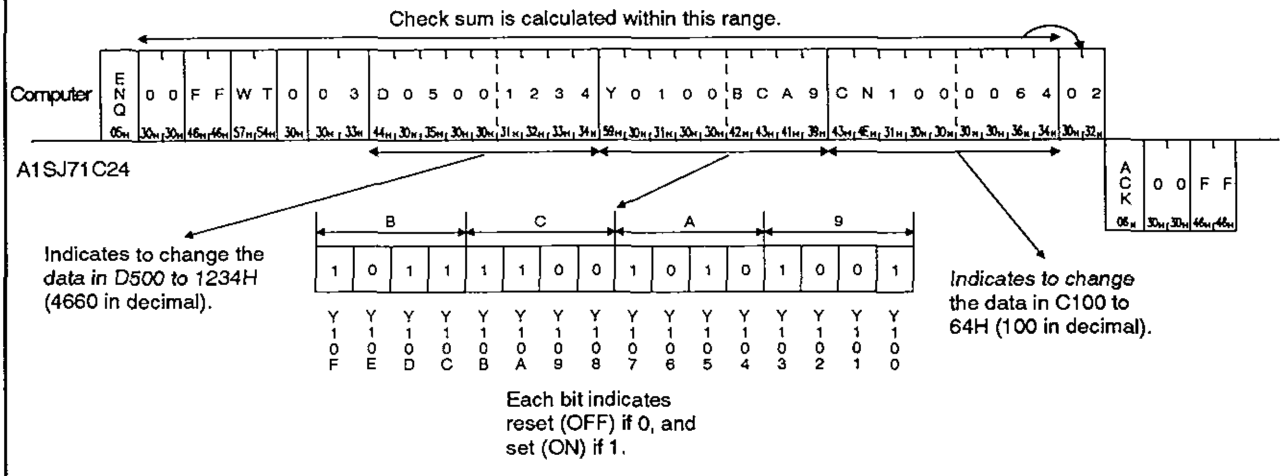
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 20 (20 units for bit devices where 1 unit corresponds to 16 points)

Designation Example

To change the present value in A1SCPU as indicated below.
(Message wait time is 0 msec)

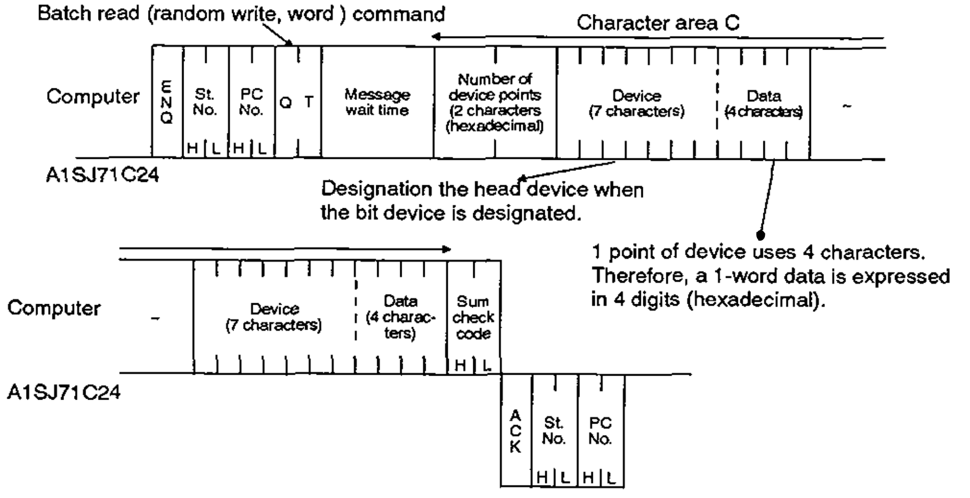


(b) Using the QT command (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



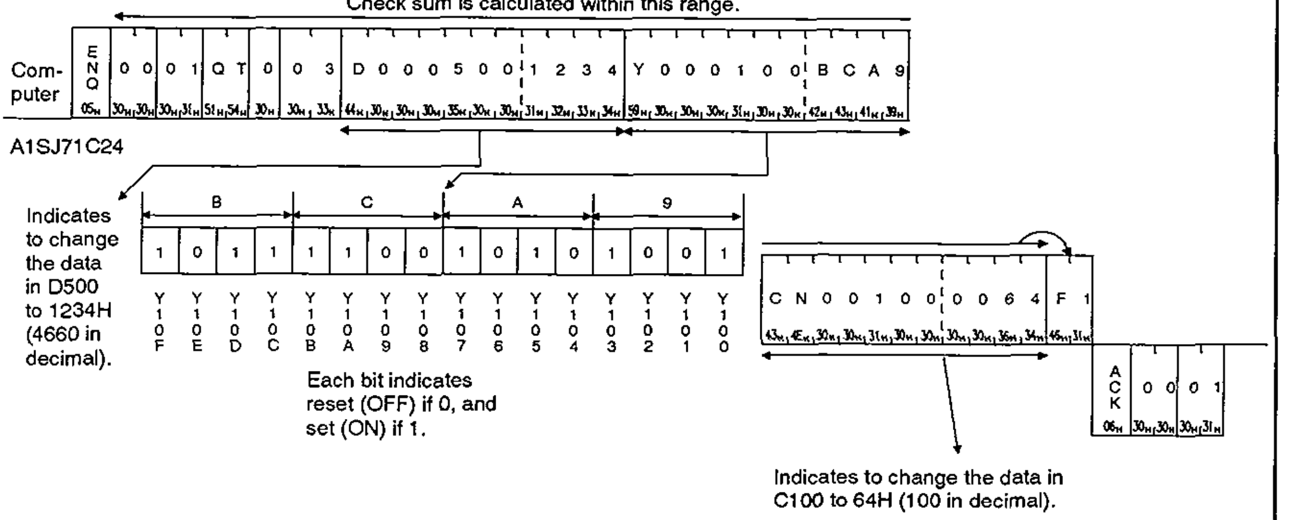
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 40 (40 units for bit devices where 1 unit corresponds to 16 points)

Designation Example

To change the present value in PC number "01" as indicated below.
(Message wait time is 0 msec)

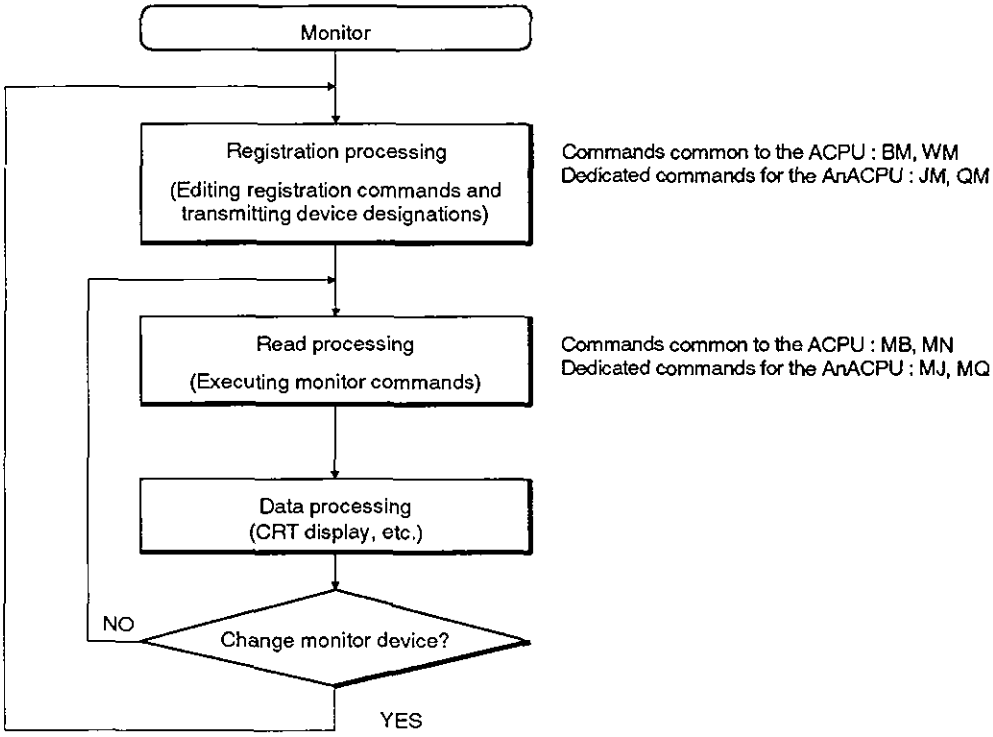


8.7.8 Monitoring device memory

Monitor data registration is the function that registers the name and the number of the device to be monitored by the computer to the A1SJ71C24. The monitor is the function that (a) reads the data content of the device registered at the time the monitor read command is executed by the computer, and (b) executes the corresponding processing such as monitoring.

The device numbers must be consecutive when the device is read using the batch read (BR, WR/JR, QR) command. However, when this function is used, it is possible to read and monitor the devices by designating the device numbers at random.

(1) Control procedure for monitoring



POINTS

(1) As the flowchart shows, monitor data registration must be executed before monitoring. Attempting to execute monitoring without registering the monitor data will cause a protocol error.

(2) The contents registered in monitor data registration are cleared when the power supply is turned OFF or the PC CPU is reset.

(3) For monitor registration, five types of registration are possible. They are device memory in bit units (BM or JM), device memory in word units (WM or QM), and the extension file register (EM).

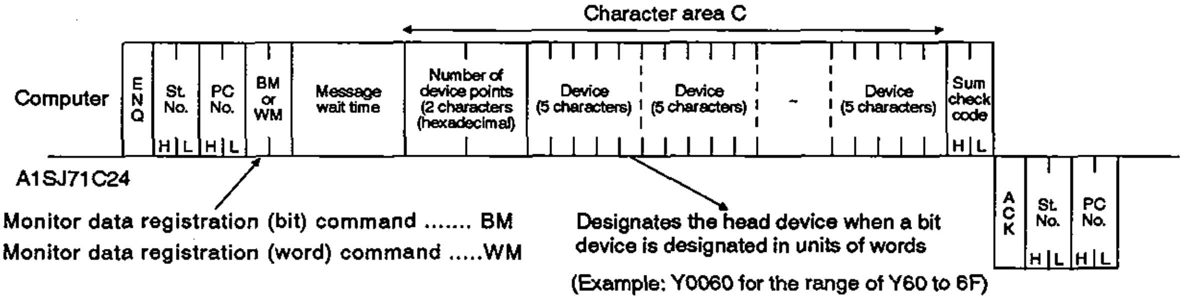
(2) Registering monitor data of device memory

(a) Using the BM or WM command (ACPU common command)

Designation Method

Designation in protocol 1 is shown below.

St. No. : Station number



POINTS

(1) To designate the device range, the following conditions must be met:

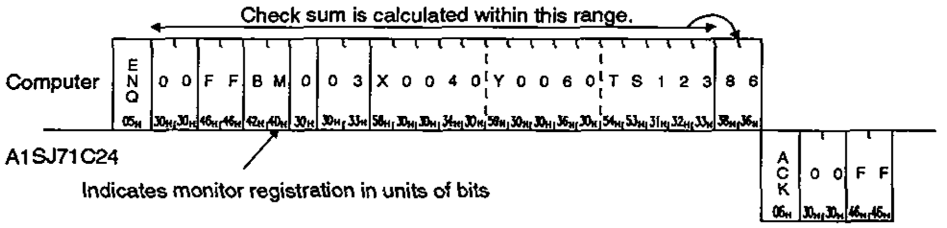
With PC CPUs other than A3HCPU, A2ACPU(S1), and A3ACPU, 1 point of device X (input) is counted as 2 points for processing.

- BM command 1 ≤ number of device points ≤ 40
- WM command 1 ≤ number of device points ≤ 20

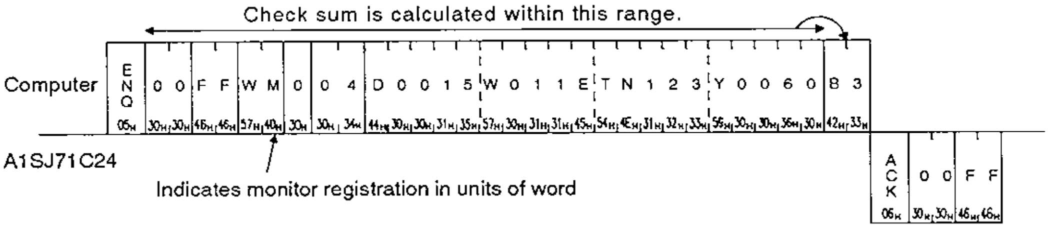
(2) With the WM command, word devices and bit devices (16 point units) can be used in combination, as shown in Example 2.

Designation Examples

Example 1:
To display monitor registration for X40, Y60, and T123 (contact) in A1SCPU.
(Message wait time is 0 msec)



Example 2 :
To register monitor data for D15, W11E, T123 (present value), and Y60 to Y6F in A1SCPU. (Message wait time is 0 msec)

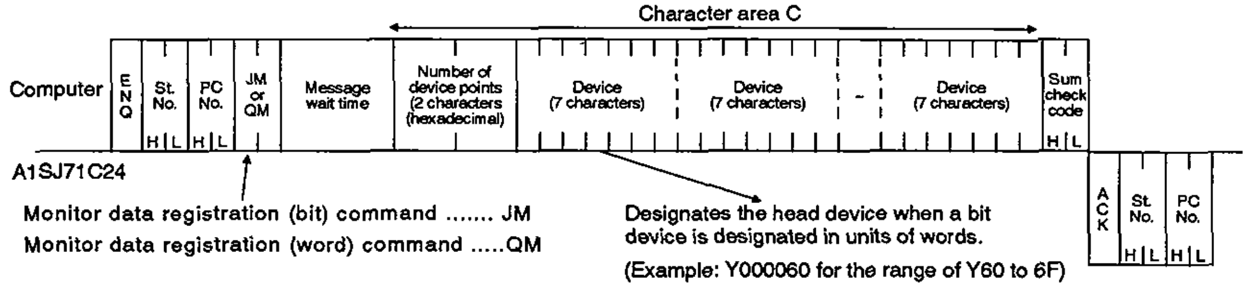


(b) Using the JM or QM commands (AnACPU dedicated commands)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



POINTS

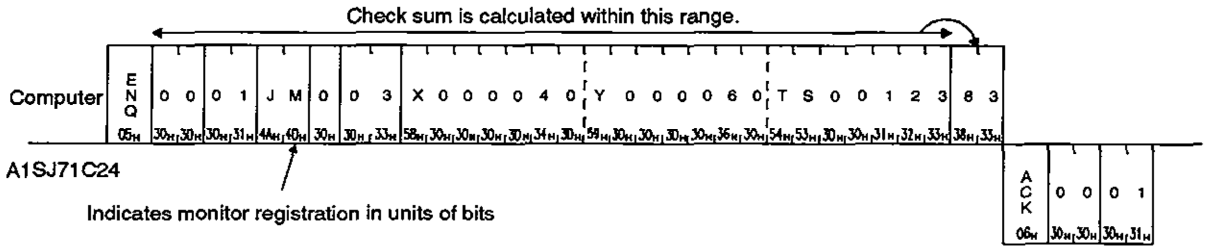
(1) To designate the device range, the following conditions must be met:

- JM command 1 ≤ number of device points ≤ 40
- QM command 1 ≤ number of device points ≤ 20

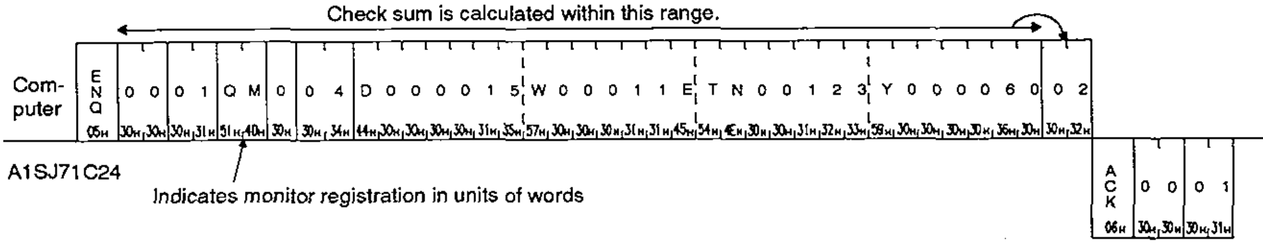
(2) With the QM command, word devices and bit devices (16-point units) can be used in combination as shown in Example 2.

Designation Examples

Example 1:
To register monitor data for X40, Y60, and T123 (contact) in PC number "01".
(Message wait time is 0 msec)



Example 2:
To register monitor data for D15, W11E, T123 (present value), and Y60 to Y6F in PC number "01". (Message wait time is 0 msec)



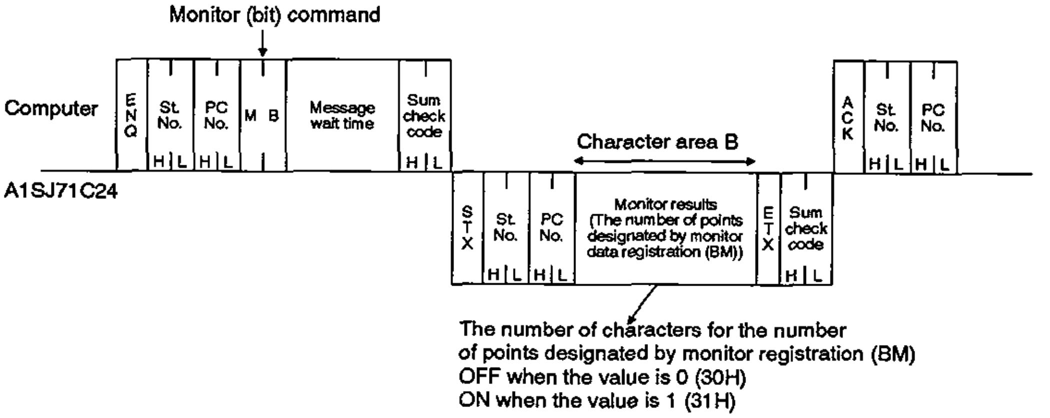
(3) Monitoring device memory in units of bits

(a) Monitoring the devices registered by the BM command (ACPU common command)

Designation Method

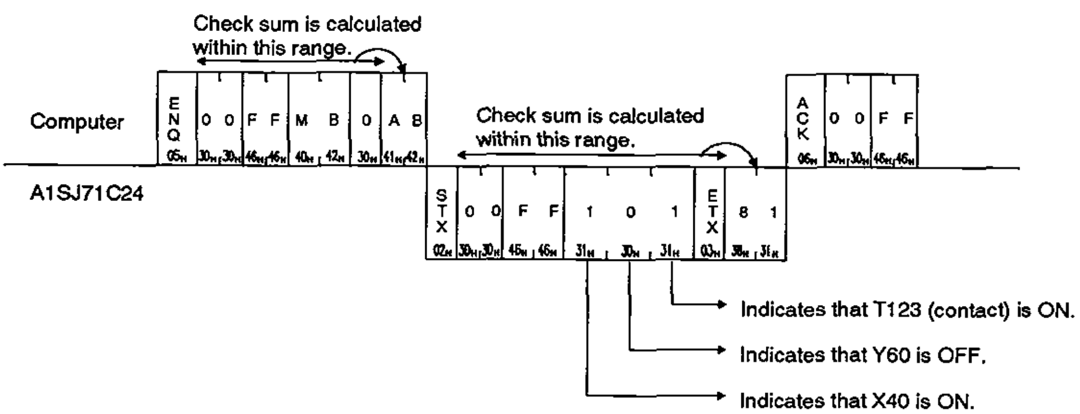
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

Monitoring is executed after registering the monitor data (bit units) in Example 1 of (2) (a)
(Message wait time is 0 msec)

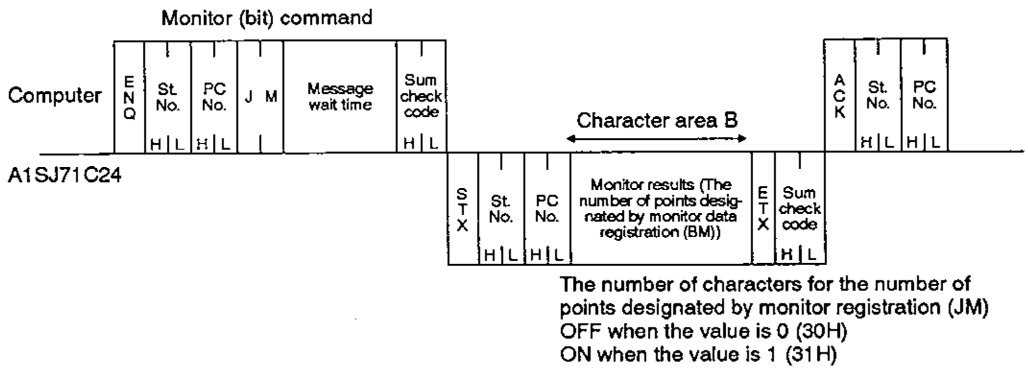


(b) Monitoring the devices registered by the JM command (AnACPU dedicated command)

Designation Method

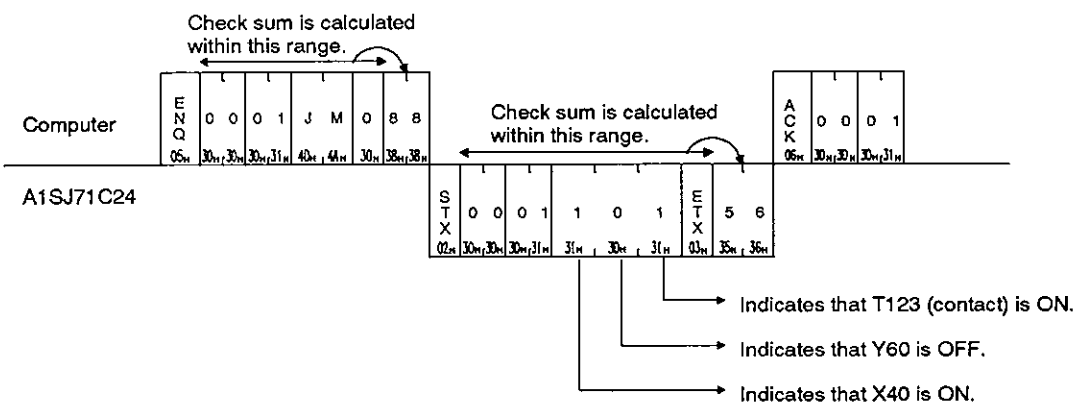
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

Monitoring is executed after registering the monitor data (bit units) in Example 1 of (2) (b)
(Message wait time is 0 msec)



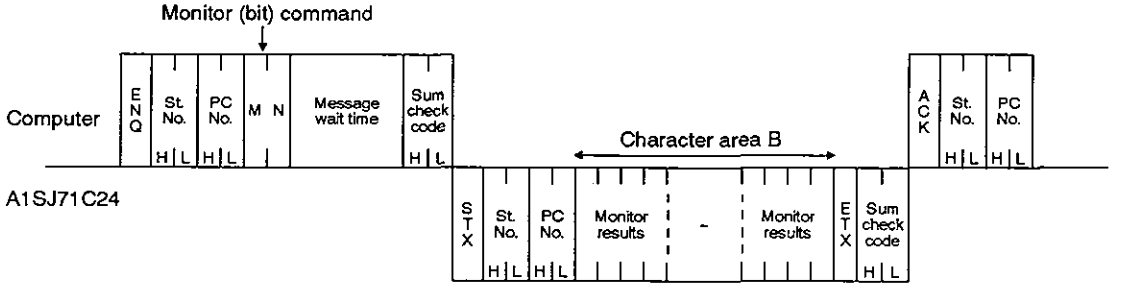
(4) Monitoring device memory in units of words

(a) Monitoring the device registered by the WM command (ACPU common command)

Designation Method

Designation in protocol 1 is shown below.

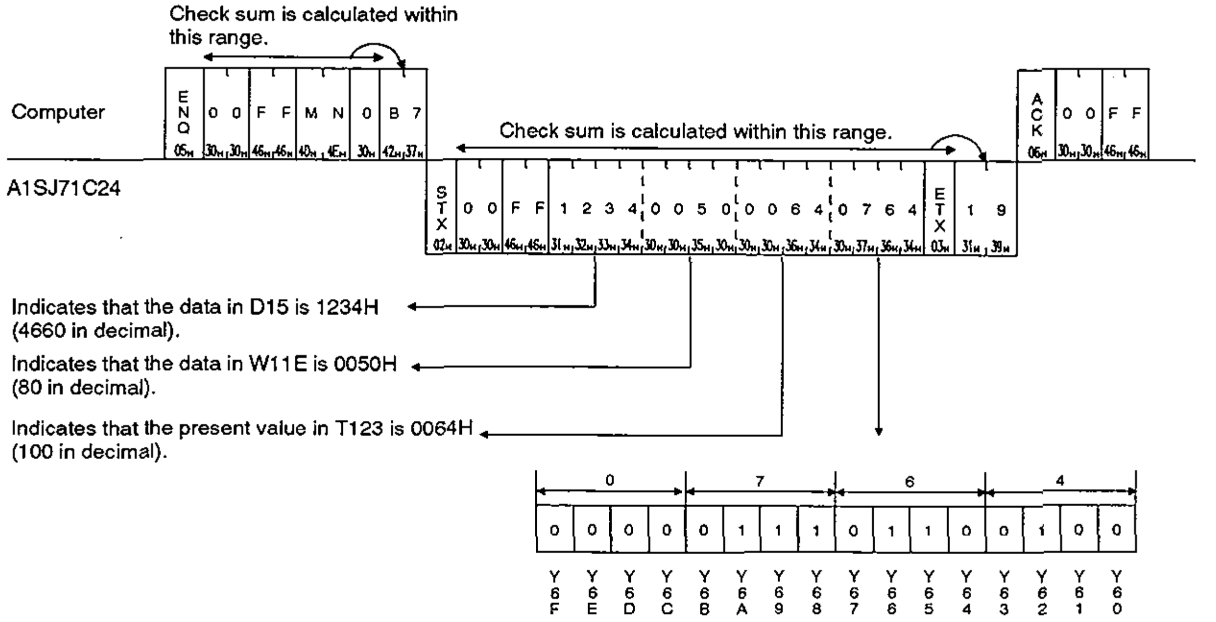
St. No. : Station number



The number of characters for the number of points designated by monitor registration (WM)
1 point of device uses 4 characters
Therefore, a 1-word data is expressed in 4 digits (hexadecimal)

Designation Example

Monitoring is executed after registering the monitor data (word units) as in Example 2 of (2) (a) (Message wait time is 0 msec)

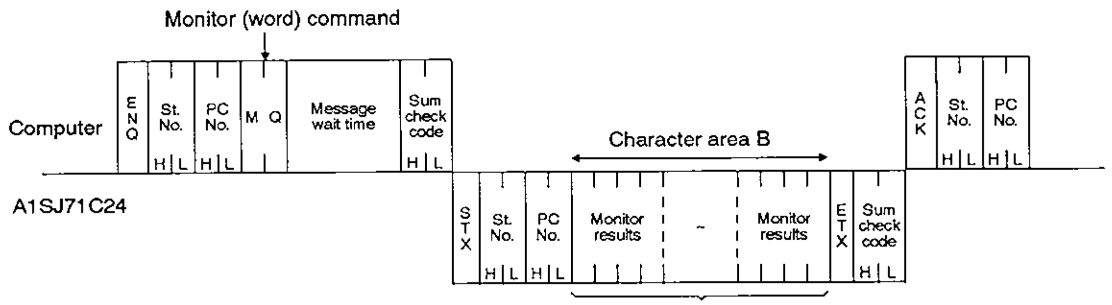


(b) Monitoring the devices registered by the QM command (AnACPU dedicated command)

Designation Method

St. No. : Station number

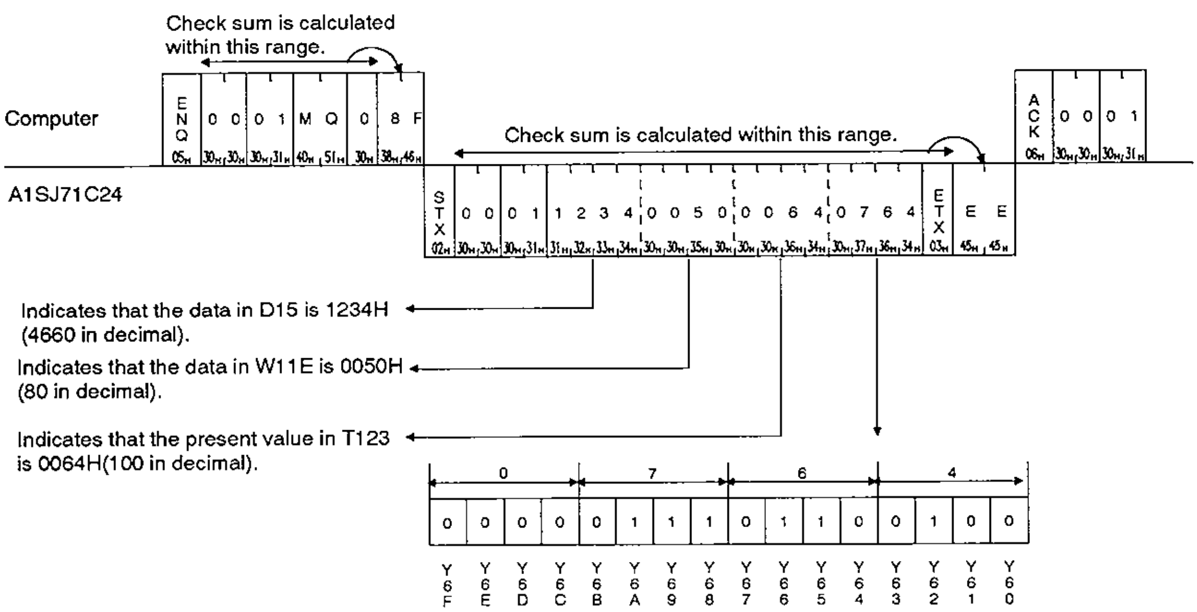
Designation in protocol 1 is shown below.



The number of characters for the number of points designated by monitor registration (QM)
1 point of device uses 4 characters
Therefore, a 1-word data is expressed in 4 digits (hexadecimal)

Designation Example

Monitoring is executed after registering the monitor data (word units) as in Example 2 of (2) (b) (Message wait time is 0 msec)



8.8 Extension File Register Read and Write

An extension file register refers to an empty area of the PC CPU user memory area used as a file register. The extension file register is used to store necessary data, results of the calculation for data processing executed using the SW0GHP-UTLPC-FN1 software package, and dedicated instructions for extension files used in the A2ACPU(S1) and A3ACPU.

8.8.1 ACPU common commands and addresses

(1) ACPU common commands used for read/write of extension file registers

Item	Command		Processing	Number of Points Processed per Communications	State of PC CPU			Access to A1SCPU	Access to PC CPU in Data Link
	Symbol	ASCII Code			During STOP	During RUN			
						SW04 ON	SW04 OFF		
Batch read	ER	45H, 52H	Reads from extension file registers (R) in units of 1 point.	64 points	o	o	o	o	o
Batch write	EW	45H, 57H	Writes to extension file registers (R) in units of 1 point.	64 points	o	o	x	o	o
Test (random write)	ET	45H, 54H	Specifies the extension file registers (R) in units of 1 point using block or device number and makes a random write.	10 points	o	o	x	o	o
Monitor data entry	EM	45H, 4DH	Sets the device numbers to be monitored in units of 1 point.	20 points	o	o	o	o	o
Monitor	ME	4DH, 45H	Monitors the extension file registers after monitor data entry.	—	o	o	o	o	o

Note : o Executable
x Not executable

(2) Extension file register addresses

(a) The extension file register comprises blocks number 0 to "n", with "n" varying according to the memory cassette. Block number "0" contains the number of points designated by the PC CPU parameters and each block with numbers "1" to "n" has 8192 points of registers.

Read/write is possible in the range of parameters designated in block number 0.

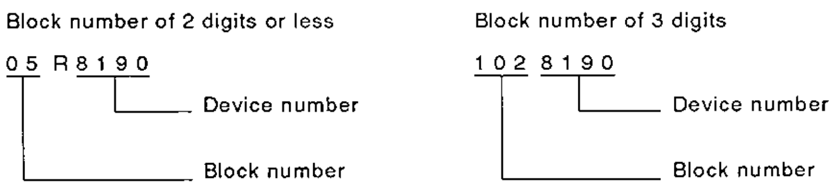
(b) The range of block numbers which can be designated varies according to the type of memory cassette and the PC CPU parameter setting.

The UTLP-FN1 Operating Manual or A2A(S1)/A3ACPU User's Manual give details.

(c) Each address is designated in 7 characters consisting of the block and device numbers.

- Block number of 2 digits or less:
  "Block number (2 digits)" + "R" + "Device number (4 digits)"
- Block number of 3 digits:
  "Block number (3 digits)" + "Device number (4 digits)

Example:



8.8.2 AnACPU dedicated commands and device numbers

(1) The AnACPU dedicated commands used for direct read and direct write of extension file registers are described below.

These dedicated commands are used to access the extension file register of block numbers 1 to 256 by directly designating the address, which begins with address 0 in block number 1, as the device number. The address numbers used to access the extension·file register go from 0 to "the usable number of blocks x 8192 points".

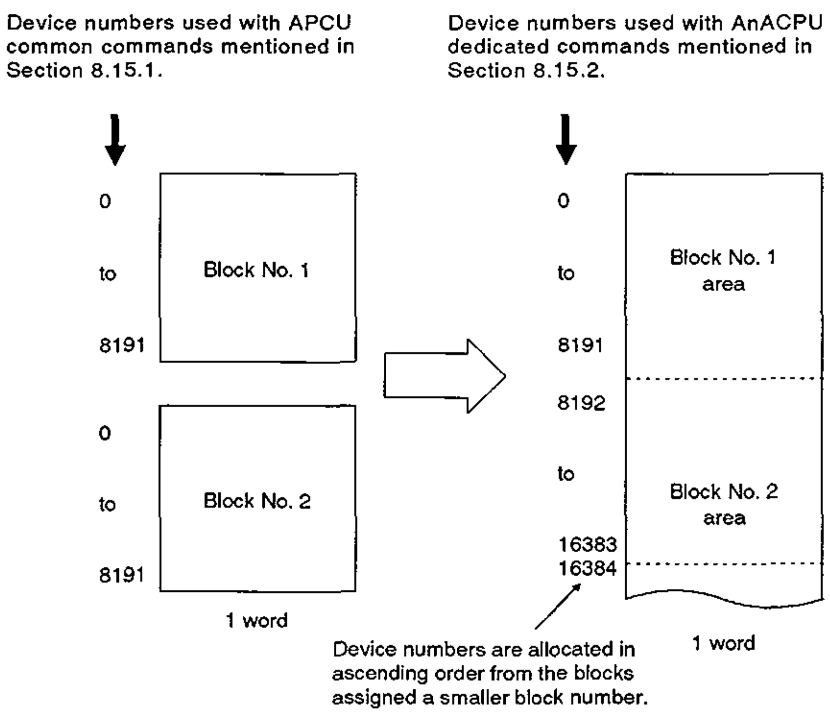
Item	Command		Processing	Number of Points Processed per Communications	State of PC CPU			Access to A1SCPU	Access to PC CPU in Data Link
	Symbol	ASCII Code			During STOP	During RUN			
						SW04 ON	SW04 OFF		
Direct read	NR	4EH, 52H	Reads in units of points (words) by designating the extension file register in successive numbers.	64 points	o	o	o	x	o
Direct write	NW	4EH, 57H	Writes data to the extension file register in units of points (words) by designating the extension file register in successive numbers.	64 points	o	o	x	x	o

Note : o Executable
x ....Not executable

(2) Device numbers of extension file registers

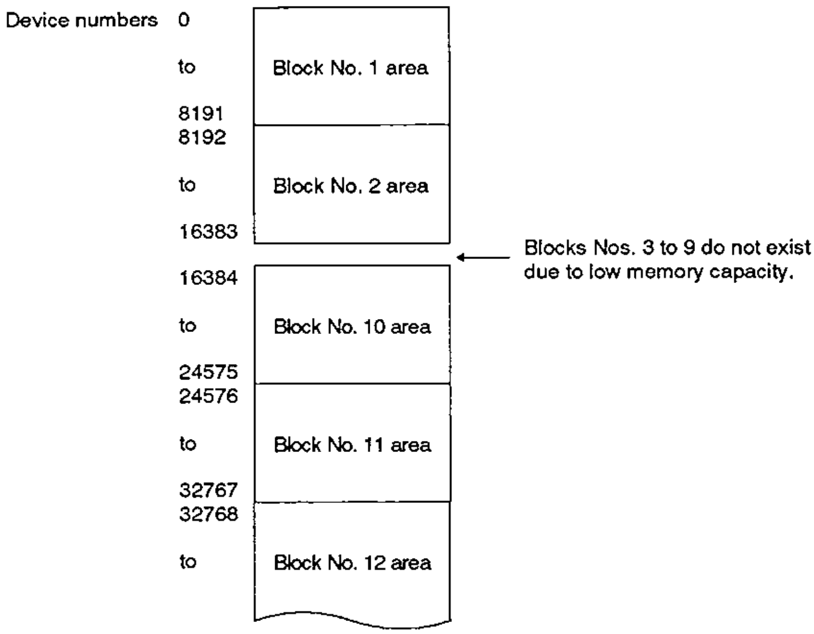
(a) Device number range

Range: 0 through [(the number of usable blocks x 8192) - 1]



The device numbers that can be designated vary according to the type of memory cassette and the PC CPU parameter setting. (The UTLP-FN1 Operating Manual or the A2A(S1)/A3A CPU User's Manual give details.)

For block numbers that do not exist in the memory cassette, device numbers are not allocated. In this case, the device numbers are allocated as indicated below, skipping non-existent block numbers.



(b) A device number is designated in 7 characters.

Designation example 1:
To designate R10 in block number 1:

0000010

Designation example 2:
To designate R8 in block number 2:

0008200

A blank code (20H) can be used to express leading zeros (the underlined 0s in <u>000</u>8200).

POINTS

(1) The AnACPU dedicated commands NR and NW can only be used for read/write operations at the extension file registers of block numbers 1 to 256.

They can be used regardless of the parameter's file register setting.

(2) Use the commands described in Section 8.15.1 to access the parameter set file registers (R) or to access a file register by designating a block number.

(3) The following equation is used to calculate the head device number to be designated with the AnACPU dedicated commands NR and NW. (To designate device number "m" (0 to 8191) in the "n"th block (n ≥ 1))

Head device number = (n–1) x 8192 + m

REMARK

The range of device numbers (up to the 28th block) that can be designated with the NR or NW commands is shown below.

Device No.	Objective Block		Device No.	Objective Block	
0 to 8191	1st block	R0 to R8191	114688 to 122879	15th block	R0 to R8191
8192 to 16383	2nd block	R0 to R8191	122880 to 131071	16th block	R0 to R8191
16384 to 24575	3rd block	R0 to R8191	131072 to 139263	17th block	R0 to R8191
24576 to 32767	4th block	R0 to R8191	139264 to 147455	18th block	R0 to R8191
32768 to 40959	5th block	R0 to R8191	147456 to 155647	19th block	R0 to R8191
40960 to 49151	6th block	R0 to R8191	155648 to 163839	20th block	R0 to R8191
49152 to 57343	7th block	R0 to R8191	163840 to 172031	21st block	R0 to R8191
57344 to 65535	8th block	R0 to R8191	172032 to 180223	22nd block	R0 to R8191
65536 to 73727	9th block	R0 to R8191	180224 to 188415	23rd block	R0 to R8191
73728 to 81919	10th block	R0 to R8191	188416 to 196607	24th block	R0 to R8191
81920 to 90111	11th block	R0 to R8191	196608 to 204799	25th block	R0 to R8191
90112 to 98303	12th block	R0 to R8191	204800 to 212991	26th block	R0 to R8191
98304 to 106495	13th block	R0 to R8191	212992 to 221183	27th block	R0 to R8191
106496 to 114687	14th block	R0 to R8191	221184 to 229375	28th block	R0 to R8191

8.8.3 Precautions during extension file register read/write

(1) The extension file register is not used by A1 and A1NCPU.

This function is not available during communications between A1 or A1NCPU and the PC CPU.

(2) Some types of memory cassette loaded to the PC CPU are unable to detect an error (character area error 06H) if an attempt is made to read or write after specifying a block number which does not exist. In this case, data which is read may not be correct and writing such incorrect data may destroy the PC CPU user memory.

Always check the type of memory cassette and the parameter settings before using this function.

Type of Memory Cassette	Block Numbers Which do not Cause a Character Area Error (06H)		
	A0J2H, A2, A3CPU	A2NCPU, A3NCPU	A3H, A2A (S1) A3ACPU
A3NMCA-12	No. 10, No. 11		
A3NMCA-18	—	No. 10 to No. 28	
A3NMCA-24	—	No. 13 to No. 20	No. 13 to No. 28
A3NMCA-40	—		No. 21 to No. 28

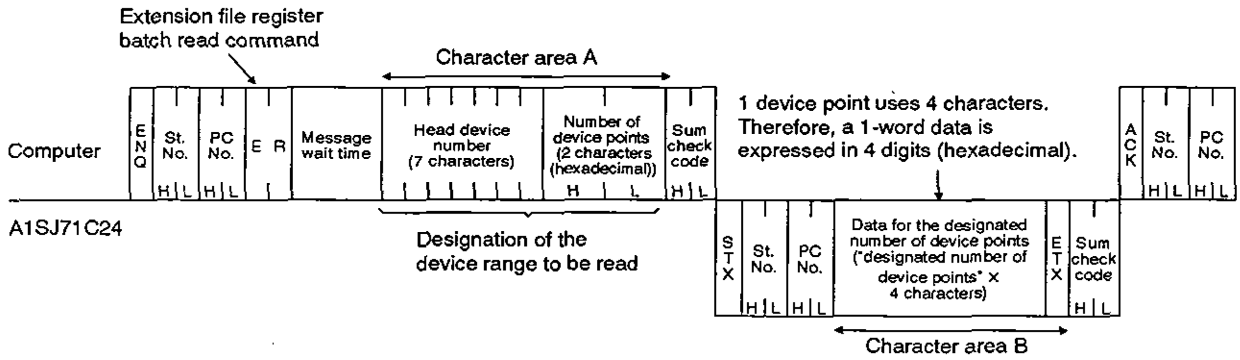
The UTLP-FN1 Operating Manual or the A2A(S1)/A3ACPU User's Manual give details.

8.8.4 Batch read of the extension file register (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



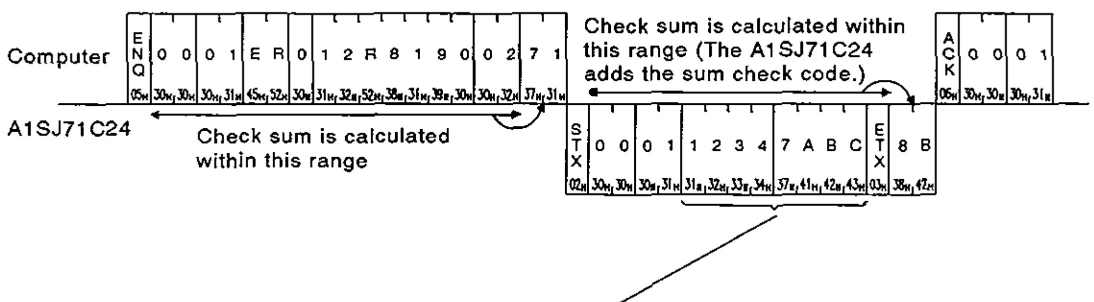
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64
- (Head device number) + (number of device points) ≤ maximum device number

Designation Example

To read the data at 2 points of R8190 and R8191 of extension file register block number 12 in PC number "01". (Message wait time is 0 msec)



Indicates that:

The content of R8190 of block Number 12 is 1234H (4660 in decimal)

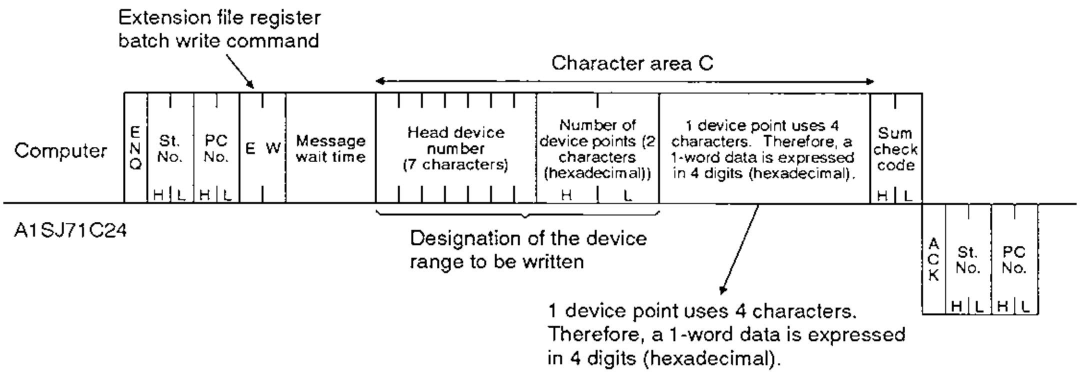
The content of R8191 of block Number 12 is 7ABCH (31420 in decimal)

8.8.5 Batch write of the extension file register (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



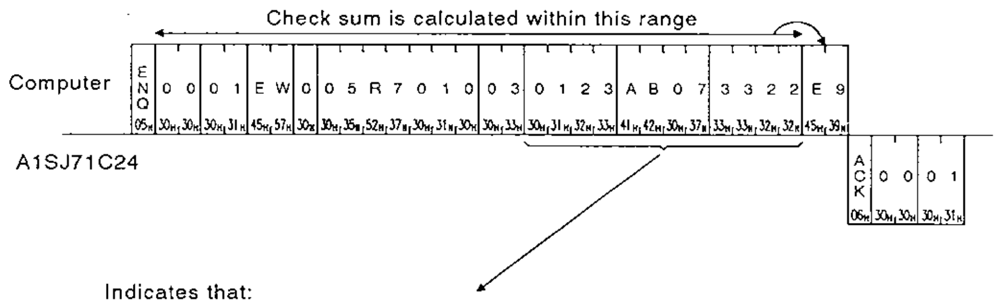
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64
- (Head device number) + (number of device points) ≤ maximum device number

Designation Example

To write data to 3 points : R7010 to R7012 in the extension file register block number 05 in PC number "01". (Message wait time is 0 msec)



Indicates that:

The content to be written to R7010 of block Number 05 is 0123H (291 in decimal)

The content to be written to R7011 of block Number 05 is AB07H (–21753 in decimal)

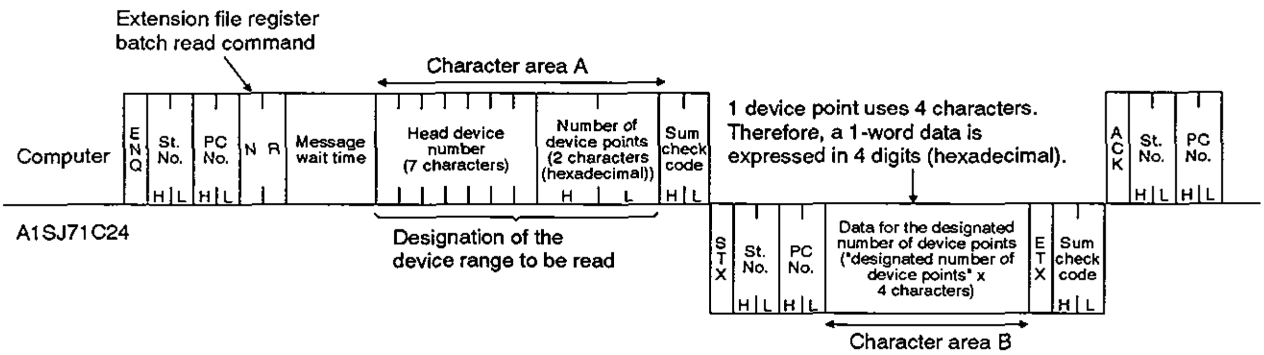
The content to be written to R7012 of block Number 05 is 3322H (13090 in decimal)

8.8.6 Direct read of the extension file register (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



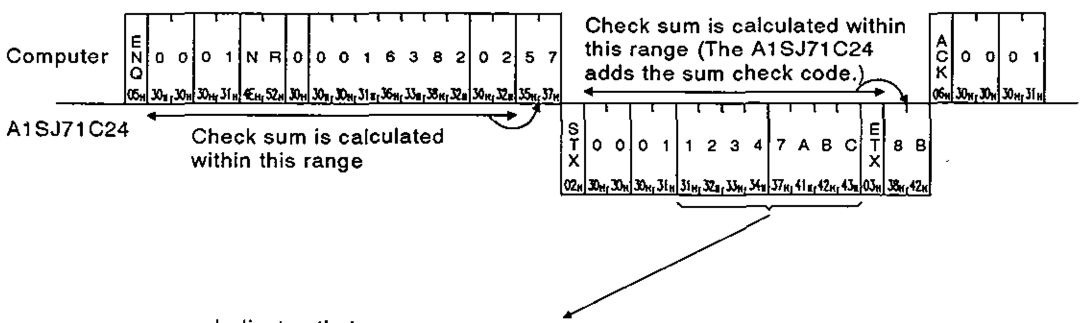
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64
- (Head device number) + (number of device points) ≤ maximum device number

Designation Example

To read the data at points of R8190 and R8191 of extension file register block number 2 in PC number "01". (Message wait time is 0 msec)



Indicates that:

The content of R8190 of block Number 2 is 1234H (4660 in decimal)

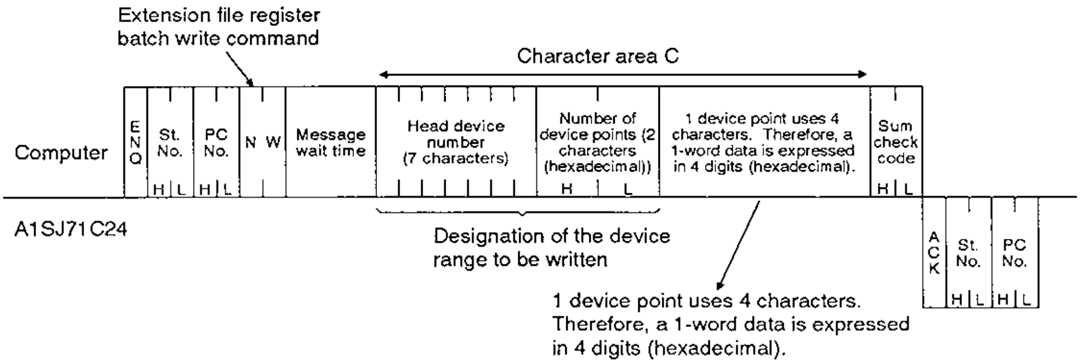
The content of R8191 of block Number 2 is 7ABCH (31420 in decimal)

8.8.7 Direct write to the extension file register (AnACPU dedicated command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



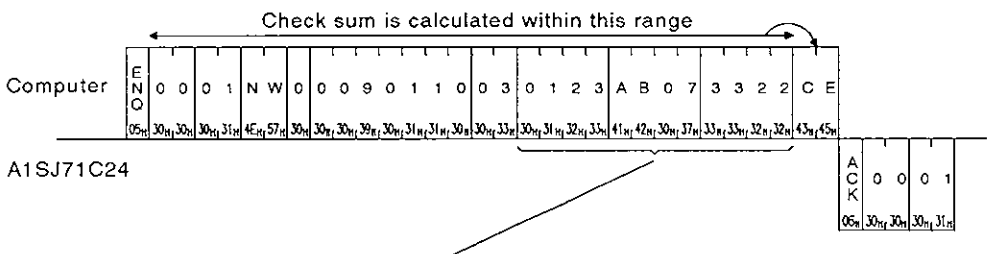
POINT

To designate the device range, the following conditions must be met:

- 1 ≤ number of device points ≤ 64
- (Head device number) + (number of device points) ≤ maximum device number

Designation Example

To write data to 3 points : R8190 and R8191 in extension file register block number 12 and R0 in block number 13, in PC number "01". Assume that extension file register block number 9 does not exist. (Message wait time is 0 msec)



Indicates that:

The content to be written to R8190 of block Number 12 is 0123H (291 in decimal)

The content to be written to R8191 of block Number 12 is AB07H (–21753 in decimal)

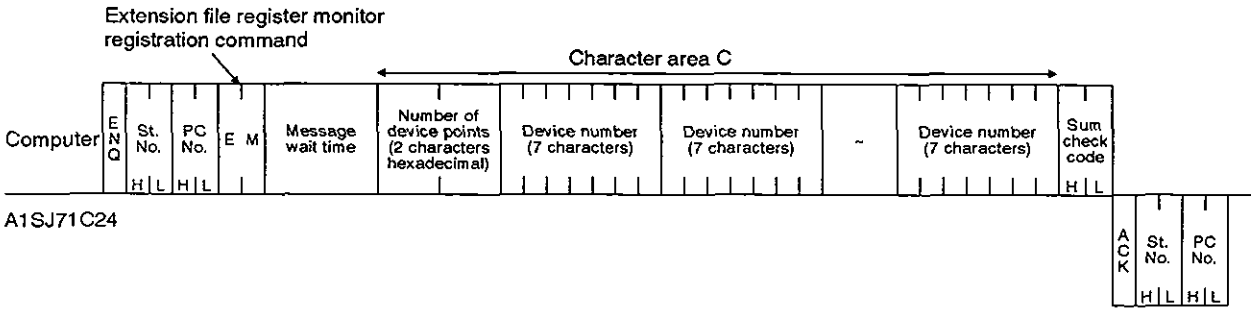
The content to be written to R0 of block Number 13 is 3322H (13090 in decimal)

(2) Registering Monitor data of the extension file register (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



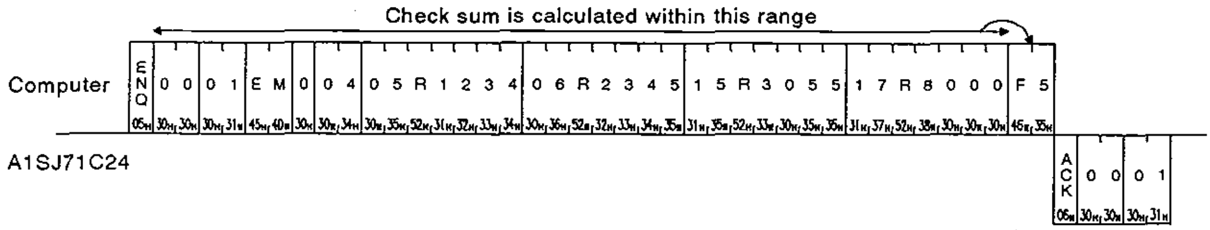
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 20

Designation Example

To register monitor data for R1234 in extension file register block number 5, R2345 in block number 6, R3055 in block number 15, and R8000 in block number 17 in PC number "01". (Message wait time is 0 msec)

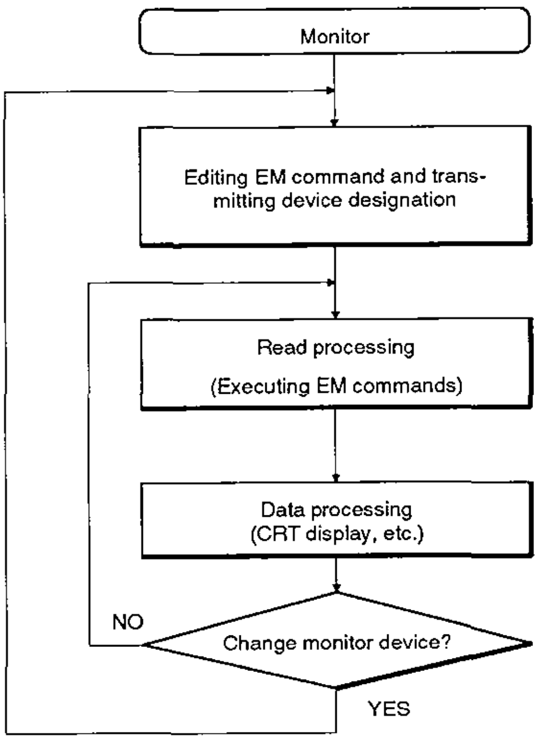


8.8.9 Monitoring the extension file register

Monitor data registration is the function that registers the name and the number of the device to be monitored by the computer to the A1SJ71C24. The monitor is the function that (a) reads the data content of the device registered at the time the monitor read command is executed by the computer, and (b) executes the corresponding processing such as monitoring.

The device numbers must be consecutive when the device is read using the batch read (ER) or direct read (NR) command. However, when this function is used, it is possible to read and monitor the devices by designating the device numbers at random.

(1) Control procedure for monitoring



POINTS

(1) As the flowchart shows, monitor data registration must be executed before monitoring. Attempting to execute monitoring without registering the monitor data will cause a protocol error.

(2) The contents registered in monitor data registration are cleared when the power supply is turned OFF or the PC CPU is reset.

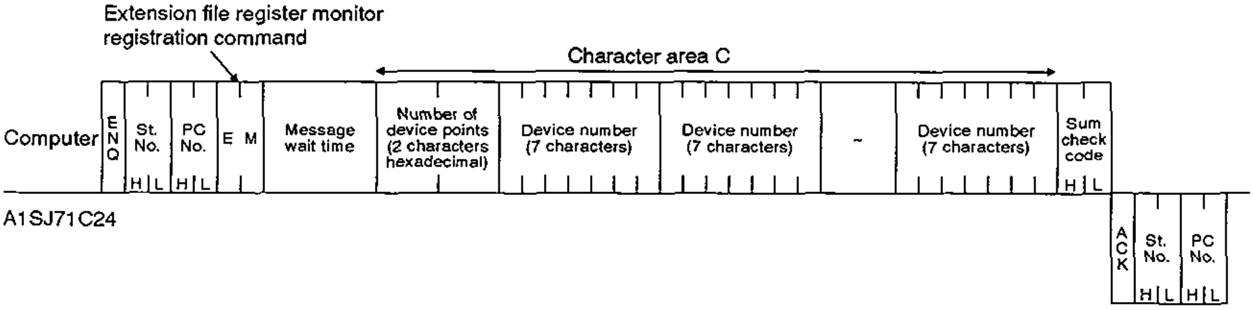
(3) For monitor registration, five types of registration are possible. They are device memory in bit units (BM or JM), device memory in word units (WM or QM) and the extension file register (EM).

(2) Registering Monitor data of the extension file register (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



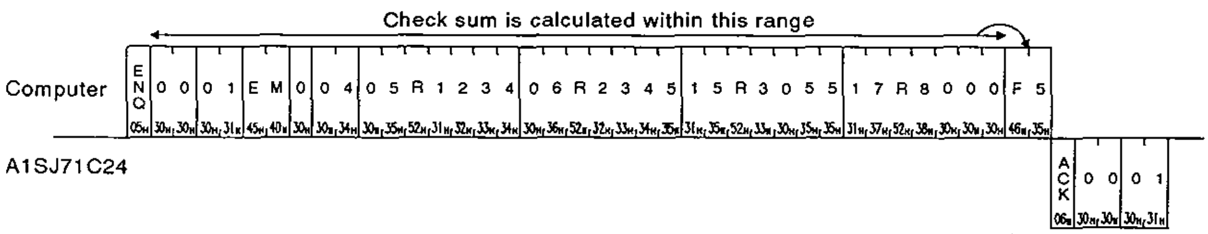
POINT

To designate the device range, the following condition must be met:

- 1 ≤ number of device points ≤ 20

Designation Example

To register monitor data for R1234 in extension file register block number 5, R2345 in block number 6, R3055 in block number 15, and R8000 in block number 17 in PC number "01". (Message wait time is 0 msec)

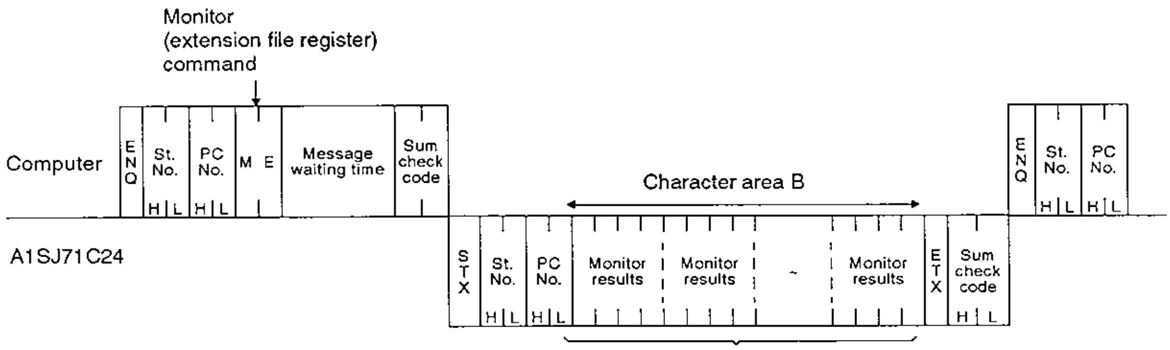


(3) Monitoring the extension file register (ACPU common command)

Designation Method

St. No. : Station number

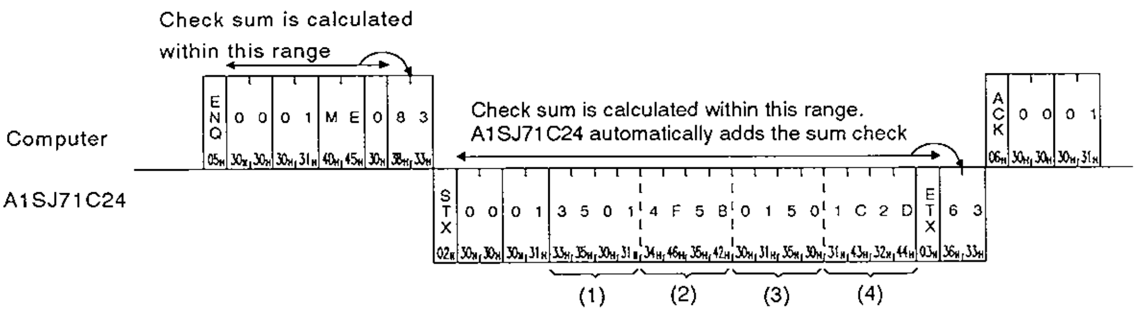
Designation in protocol 1 is shown below.



The number of characters for the number of points designated by monitor data registration (EM).
1 point of device uses 4 characters.
Therefore, a 1-word data is expressed in 4 digits (hexadecimal)

Designation Example

Monitoring after registering the monitor data (word units) as mentioned in item (2).
(Message wait time is 0 msec)



(1) the content of R1234 of extension file register block number 05 is 3501H (13569 in decimal),

(2) the content of R2345 of extension file register block number 06 is 4F5BH (20315 in decimal),

(3) the content of R3055 of extension file register block number 15 is 0150H (336 in decimal),

(4) the content of R8000 of extension file register block number 17 is 1C2DH (7213 in decimal),

8.9 Buffer Memory Read and Write

This function is used to read from and write to the A1SJ71C24 buffer memory. When this function is used, communications between the computer and A1SJ71C24 commences immediately when the computer sends a read or write request, without waiting for the PC CPU END processing. Therefore, the time T1, described in Section 8.5, is always equal to zero. The PC CPU carries out buffer memory read and write using TO and FROM instructions.

The method for specifying the control protocol, meanings, and examples for carrying out this function are shown below.

8.9.1 Commands and buffer memory

(1) ACPU common commands

Item	Command		Processing	Number of Points Processed per Communications	State of PC CPU			Access to A1SCPU	Access to PC CPU in Data Llink
						During RUN			
	Symbol	ASCII Code			During STOP	SW04 ON	SW04 OFF		
Batch read	CR	43H, 52H	Reads from buffer memory.	64 words (128 bytes)	o	o	o	o	o
Batch write	CW	43H, 57H	Writes to buffer memory.					o	o

Note : o .... Executable

(2) Buffer memory

Buffer memory addresses are 0H to 7FFH see (see Section 3.5).

One address consists of 1 word (16 bits).

Read and write are both executed in word units, regardless of the word/byte unit setting.

POINT

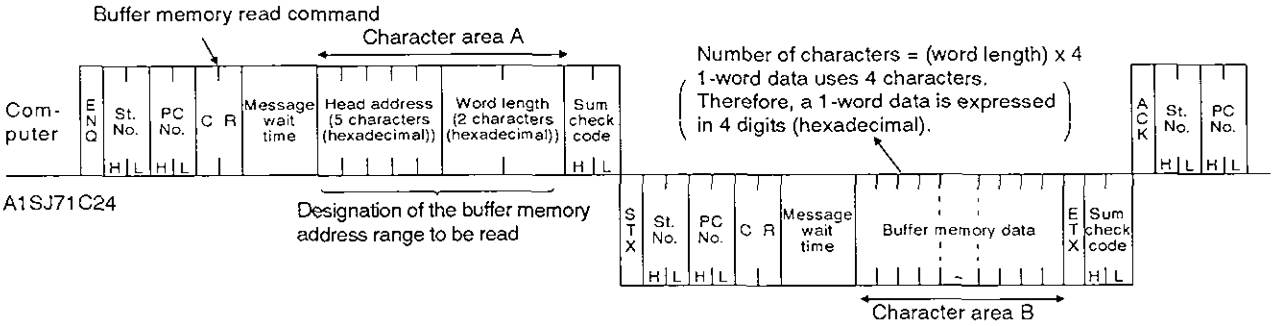
Buffer addresses 100H to 11FH comprise the special applications area. The A1SJ71C24 will not operate correctly if any operations other than those described in the following sections are executed.

8.9.2 Reading data from buffer memory (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



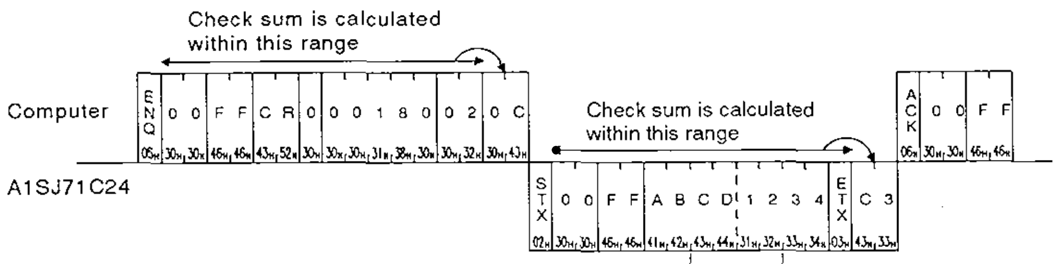
POINT

To designate the word length, the following conditions must be met:

- 1 ≤ word length ≤ 64
- *(Head address) + (word length) − 1 ≤ maximum address* number (7FFH)

Designation Example

To read 2-word data from buffer memory addresses 180H and 181H in the A1SJ71C24 which is connected to an A1SCPU:
(Message wait time is 0 msec)



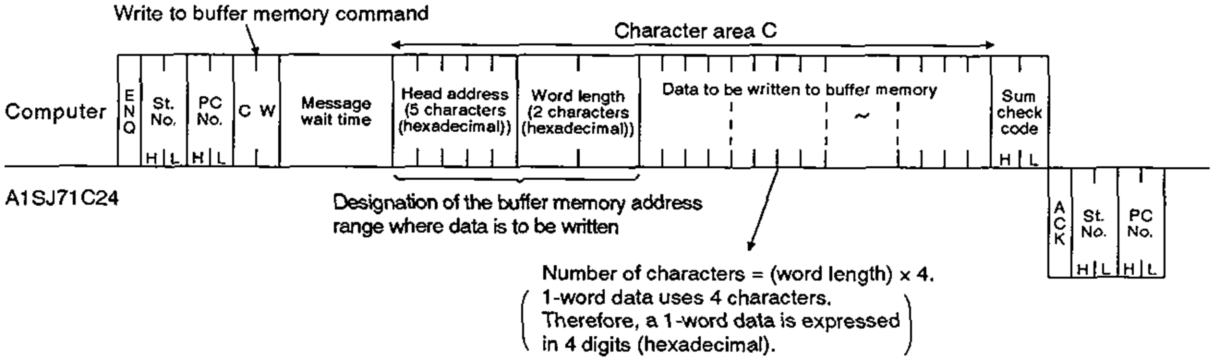
Indicates that:
The content of buffer memory address 180H is ABCDH (−21555 in decimal)
The content of buffer memory address 181H is 1234H (4660 in decimal)

8.9.3 Writing data to buffer memory (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



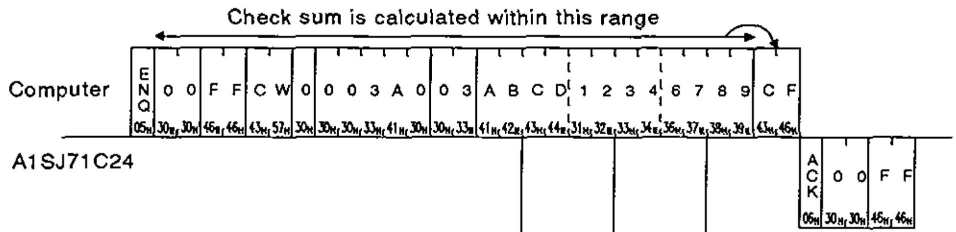
POINT

To designate the word length, the following conditions must be met:

- 1 ≤ word length ≤ 64
- (Head address) + (word length) − 1 ≤ maximum address number (7FFH)

Designation Example

To write 3-word data to buffer memory address 3A0H to 3A2H in the A1SJ71C24 which is connected to an A1SCPU.
(Message wait time is 0 msec)



Indicates that:
ABCDH (−21555 in decimal) is written to buffer memory address 3A0H
1234H (4660 in decimal) is written to buffer memory address 3A1H
6789H (26505 in decimal) is written to buffer memory address 3A2H

8.10 Special Function Module Buffer Memory Read and Write

8.10.1 Commands and designation

(1) ACPU common commands

Item	Command		Processing	Number of Points Processed per Communications	State of PC CPU			Access to A1SCPU	Access to PCCPU in Data Link
	Sym-bol	ASCII Code			During STOP	During RUN			
						SW04 ON	SW04 OFF		
Batch read	TR	54H, 52H	Reads from special function module buffer memory.	64 words (128 bytes)	o	o	o	o	o
Batch write	TW	54H, 57H	Writes to special function module buffer memory.		o	o	x	o	o

Note : o .... Executable
x .... Not executable

(2) Linkable special function modules, buffer memory head address, and *module numbers*

Special-function Module	Head Buffer Address (hexadecimal)	Module No. When Loaded in Slot 0
A1SD61 high-speed counter module	80H	01H
A1S62DA digital-analog converter module	10H	01H
A1S62RD3/4 temperature-digital converter module	10H	01H
A1S64AD analog-digital converter module	80H	01H
A1SJ71C24-R2 computer link module	400H	01H

(3) Special-function module buffer memory

The special-function module buffer memory is comprised of 16-bit (one word) addresses. Read and write of the special-function module buffer memory is executed by TO and FROM instructions transmitted between the PC CPU and special-function module.

When the computer reads from and writes to the special-function module buffer memory via the A1SJ71C24, it is done in byte units (1 address = 8 bits).

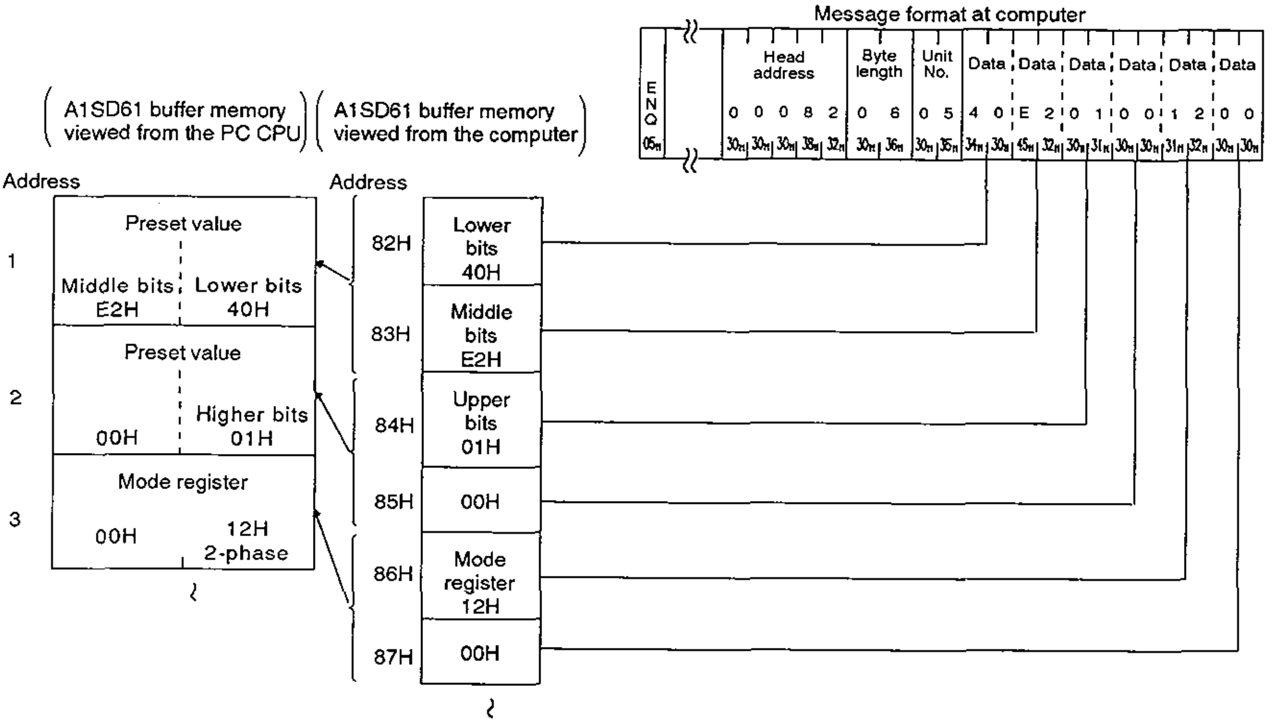
The addresses specified in the computer (hexadecimal) are converted from FROM/TO instruction addresses as shown below:

Designated address (hexadecimal) = Module head address + [(FROM/TO instruction address × 2) converted into hexadecimal]

Example: To designate A1SD61 high-speed counter module FROM/TO instruction address 1 (CH.1 preset value).

Specified address		FROM/TO instruction address 1 × 2		Head address
82H	=	2H	+	80H

The data format when the computer makes a read or write to or from the special-function module buffer memory via the A1SJ71C24, is explained below using the A1SD61 module as an example.



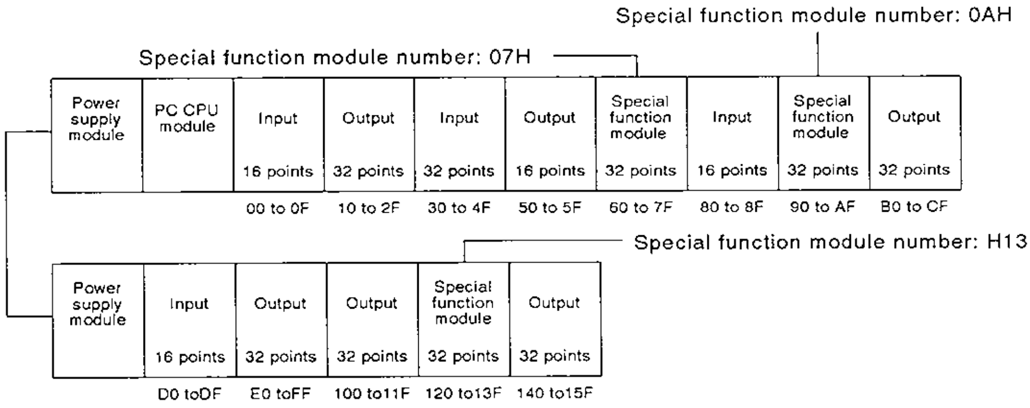
POINT

The buffer memory of each special-function module has its read and write area, read-only and write-only areas, and areas reserved for OS use, which are not available to the use. See the manual for each module before using the buffer memory.

PC CPU or special-function module errors may occur if reading or writing is not done correctly.

8.10.2 Special function module numbers using control protocols

(1) The special function module numbers designated by using control protocols are the upper 2 digits of the last special function module I/O address expressed in 3 digits.

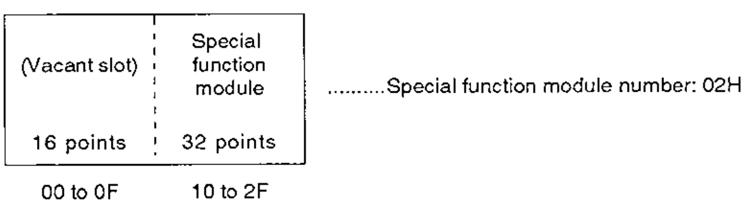


(2) Precautions with special function modules occupying two slots

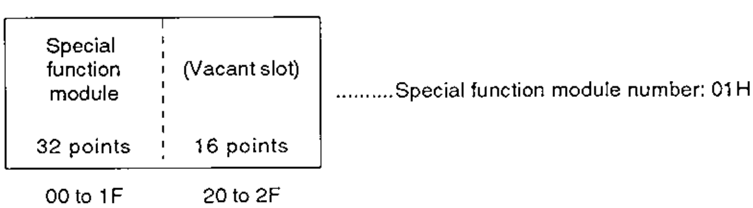
For special function modules occupying two slots, the number of points occupied by each slot is fixed for each module. The special function module number is the upper 2 digits of the last address of the slot allocated to the special function module.

The User's Manual for each special function module gives details about the allocation of slots to each module.

(a) Modules with the front slot allocated as the vacant slot (AD72, A84AD, etc.)



(b) Modules with the rear slot allocated as the empty slot (A61LS, etc.)



(c) Modules with the special function module allocation and I/O allocation mixed (A81CPU, etc.)

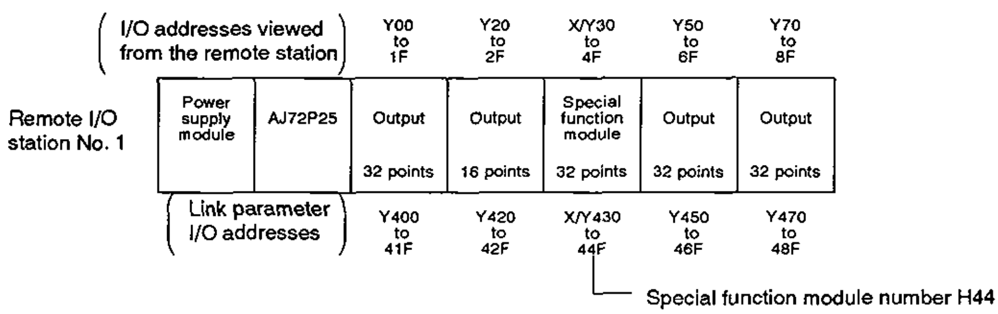
Special function module	Input module
64 points	64 points
00 to 3F	40 to 7F

..........Special function module number: 03H

(3) Module numbers of special-function modules at MELSECNET remote I/O stations

The module numbers of special function modules at MELSECNET remote stations are determined by link parameters setting at the MELSECNET master station.

L/R	M ← L		M → R	M ← R	M → L/R		M ← L/R	
NO.	B	W	W	W	Y	X/Y	X	Y/X
R1	----	----	29C–309	0F9–15E	400–48F	000–08F	430–44F	030–04F
R2	----	----	215–24F	080–0A3	510–67F	010–17F	500–65F	000–15F
R3	----	----	1B6–214	15F–1B5	270–32F	050–10F	220–28F	000–06F
	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-
	-	-	-	-	-	-	-	-

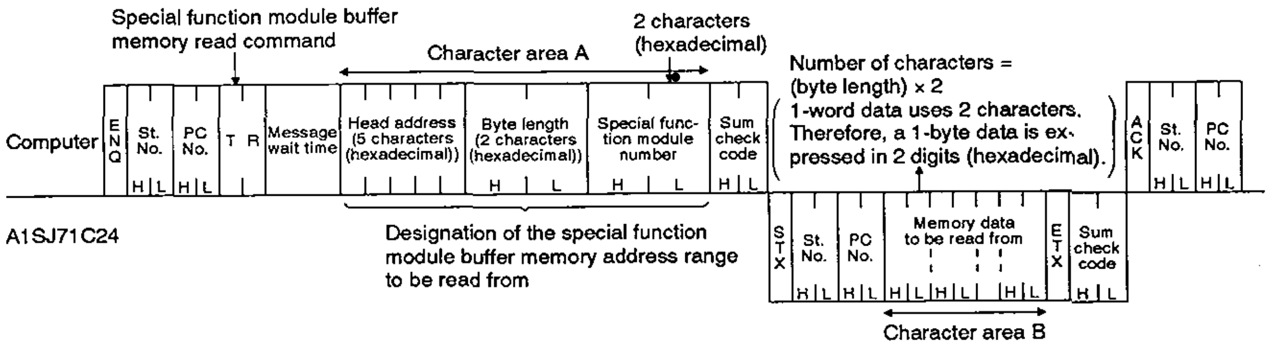


8.10.3 Reading data from the special-function module buffer memory (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



POINTS

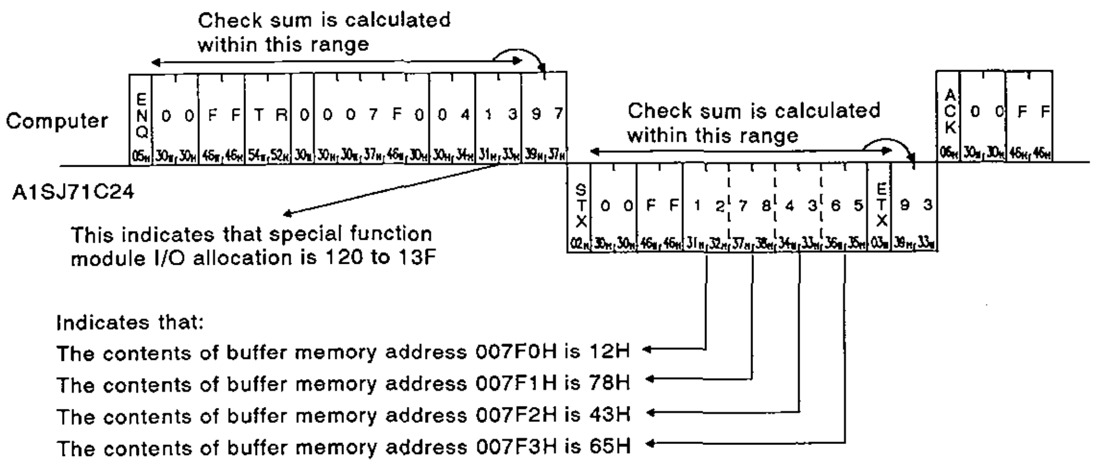
(1) To designate the byte length, the following condition must be met:

- 1 ≤ byte length ≤ 128

(2) With some special function modules, 2 or 3 bytes are used to express the data. Therefore, designate the byte length by referring to the manuals for each individual module.

Designation Example

To read the data from buffer memory address 07F0H to 07F3H (4 bytes) of the special-function module (module number 13H) loaded at I/O numbers 120 to 13F in A1SCPU. (Message wait time is 0 msec)

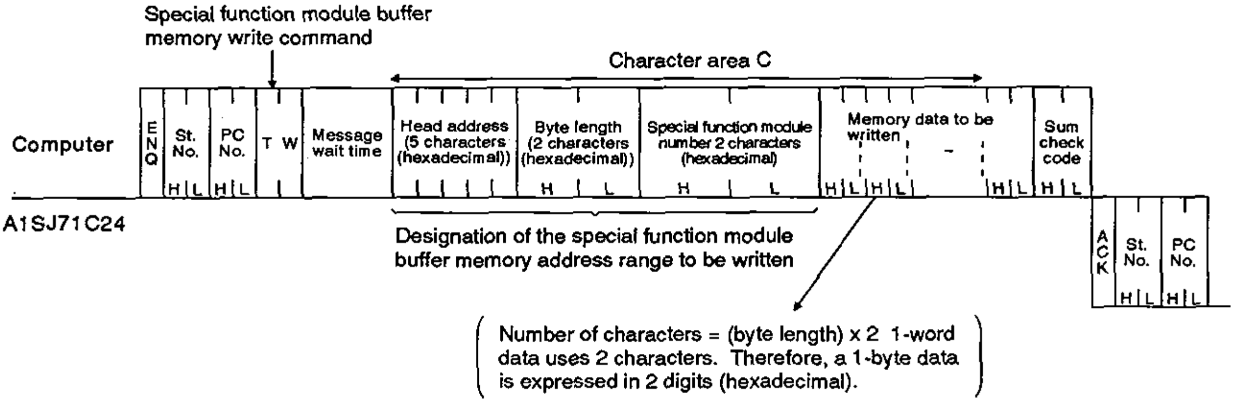


8.10.4 Writing data to the special function module buffer memory (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



POINTS

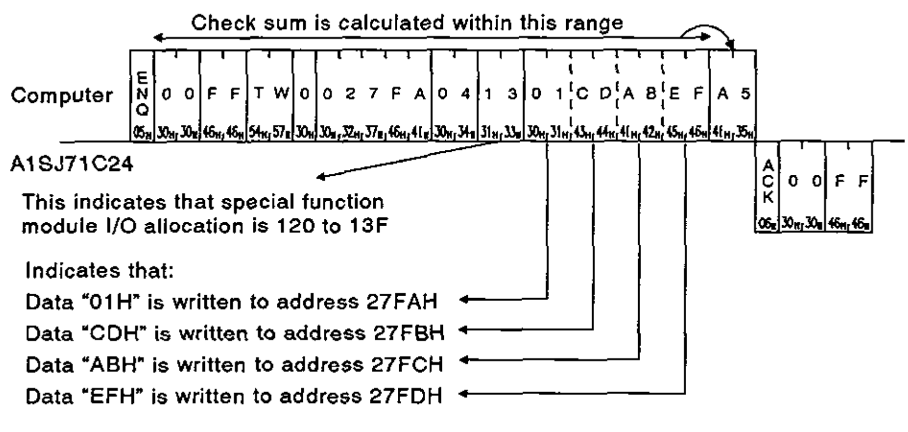
(1) To designate the byte length, the following condition must be met:

- 1 ≤ byte length ≤ 128

(2) With some special function modules, 2 or 3 bytes are used to express the data. Therefore, designate the byte length by referring to the manuals for each individual module.

Designation Example

To write the data to buffer memory address 27FAH to 27FDH (4 bytes) of the special-function module (module number 13H) loaded at I/O numbers 120 to 13F in A1SCPU.
(Message wait time is 0 msec)



8.11 Remote Run/Stop of PC CPU and Reading PC CPU Model Name

8.11.1 Commands

(1) ACPU common commands

Item	Command		Processing	State of PC CPU			Access to A1SCPU	Access to PC CPU in Data Link
	Symbol	ASCII Code		During STOP	During RUN			
					SW04 ON	SW04 OFF		
Remote RUN	RR	52H, 52H	Requests remote RUN of PC CPU.	o	o	o	o	o
Remote STOP	RS	52H, 53H	Requests remote STOP of PC CPU.	o	o	o	o	o
PC CPU modle mode	PC	50H, 43H	Reads if the PC CPU is model A1N, A2N, A3N, A3H or AJ72P25/R25.	o	o	o	o	o

Note : o....... Executable

8.11.2 Remote RUN/STOP

(1) Remote RUN/STOP control

(a) RUN, STOP, PAUSE and STEP-RUN states are produced by the following combinations of PC CPU key switch positions and computer commands.

		PC CPU Key Switch Position			
		RUN	**STOP**	**PAUSE**	**STEP-RUN**
Command from computer	Remote RUN	RUN	STOP	PAUSE	STEP-RUN
	Remote STOP	STOP	STOP	STOP	STOP

REMARKS

(a) When a PC CPU is stopped by the remote STOP command given by an external computer, that PC CPU cannot be put into the RUN state by the computer connected to the PC CPU.

(b) The clearing of data memories on receiving a remote RUN instruction depends on the states of special relays M9016 and M9017 as shown below.

Special Relay		Data Memory State
M9016	**M9017**	
OFF	OFF	PC CPU enters the RUN state without clearing remote STOP data.
OFF	ON	Remote STOP data is cleared outside the latch range set in parameters. (In this case, Link X image is not cleared.)
ON	ON/OFF	PC CPU enters the RUN state after data memory is cleared.

REMARK

Always reset special relays M9016 and M9017 when data memory clearing is not required.

POINT

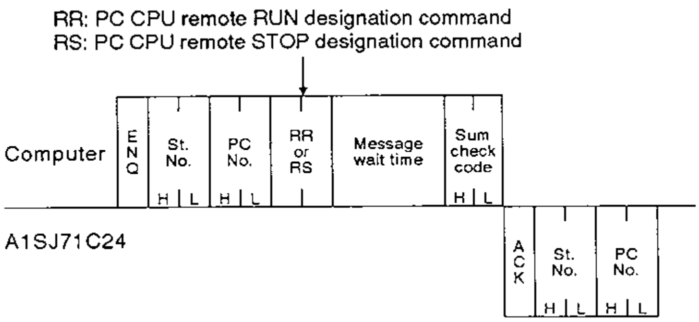
After operations remote RUN/STOP control from the computer are completed, the remote data will be lost if the power supply is turned OFF or the PC CPU is reset.

(2) Remote RUN/STOP designations and designation examples (ACPU common command)

Designation Method

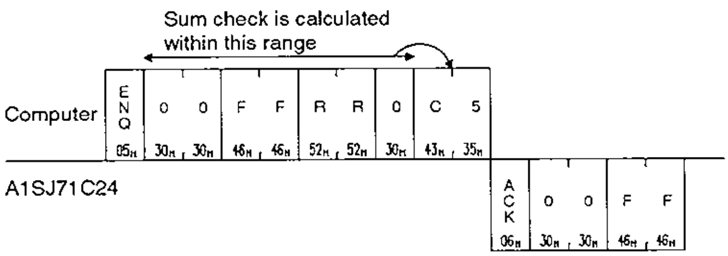
St. No. : Station number

Designation in protocol 1 is shown below.

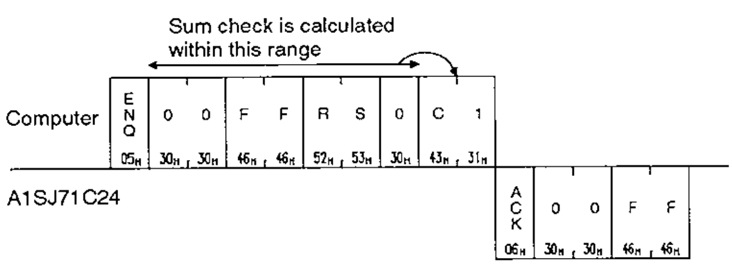


Designation Examples

Example 1: Remote RUN control of A1SCPU (Message wait time is 0 msec)



Example 2: Remote STOP control of A1SCPU (Message wait time is 0 msec)



8.11.3 Reading PC CPU model name

(1) PC CPU model name and corresponding codes

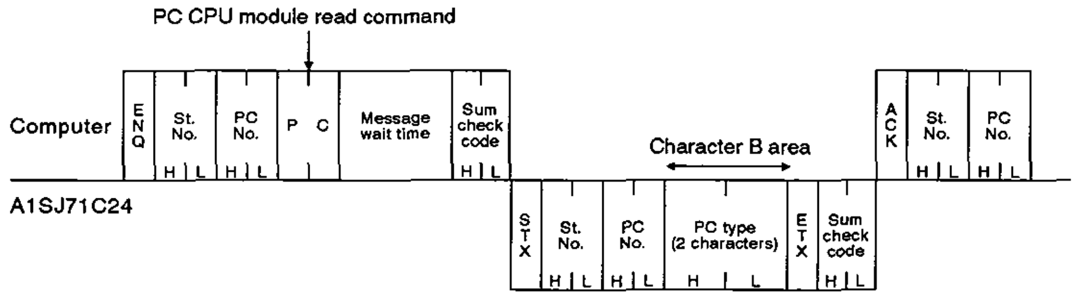
PC CPU Model Name	Code To Be Read (Hexadecimal)	PC CPU Model Name	Code To Be Read (Hexadecimal)
A0J2HCPU	98H	A3CPU, A3NCPU	A3H
A1CPU, A1NCPU	A1H	A3ACPU	94H
A2CPU(-S1), A2NCPU(-S1)	A2H	A3HCPU, A3MCPU	A4H
A2ACPU	92H	A73CPU	A3H
A2ACPU-S1	93H	AJ72P25/R25	ABH
A1SCPU	98H	A2CCPU	9AH

(2) Reading PC CPU model name (ACPU common commands)

Designation Method

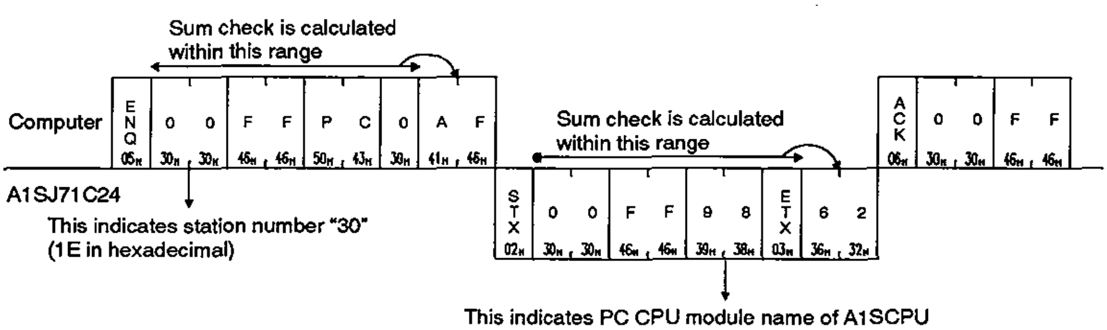
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

To read PC CPU model name at station number "0" (Message wait time is 0 msec)



8.12 Program Read/Write

This function is used to transfer all types of programs (main and subsequence programs, microcomputer main and sub programs), parameters and comment data from the PC CPU and store them in the computer. The computer then carries out the appropriate controls by writing programs, parameters, and comment data to the PC CPU.

8.12.1 Precautions during program read/write

(1) When reading programs that have been written to the PC CPU, read all sequence programs, microcomputer programs, parameter data, and comment data from all areas.

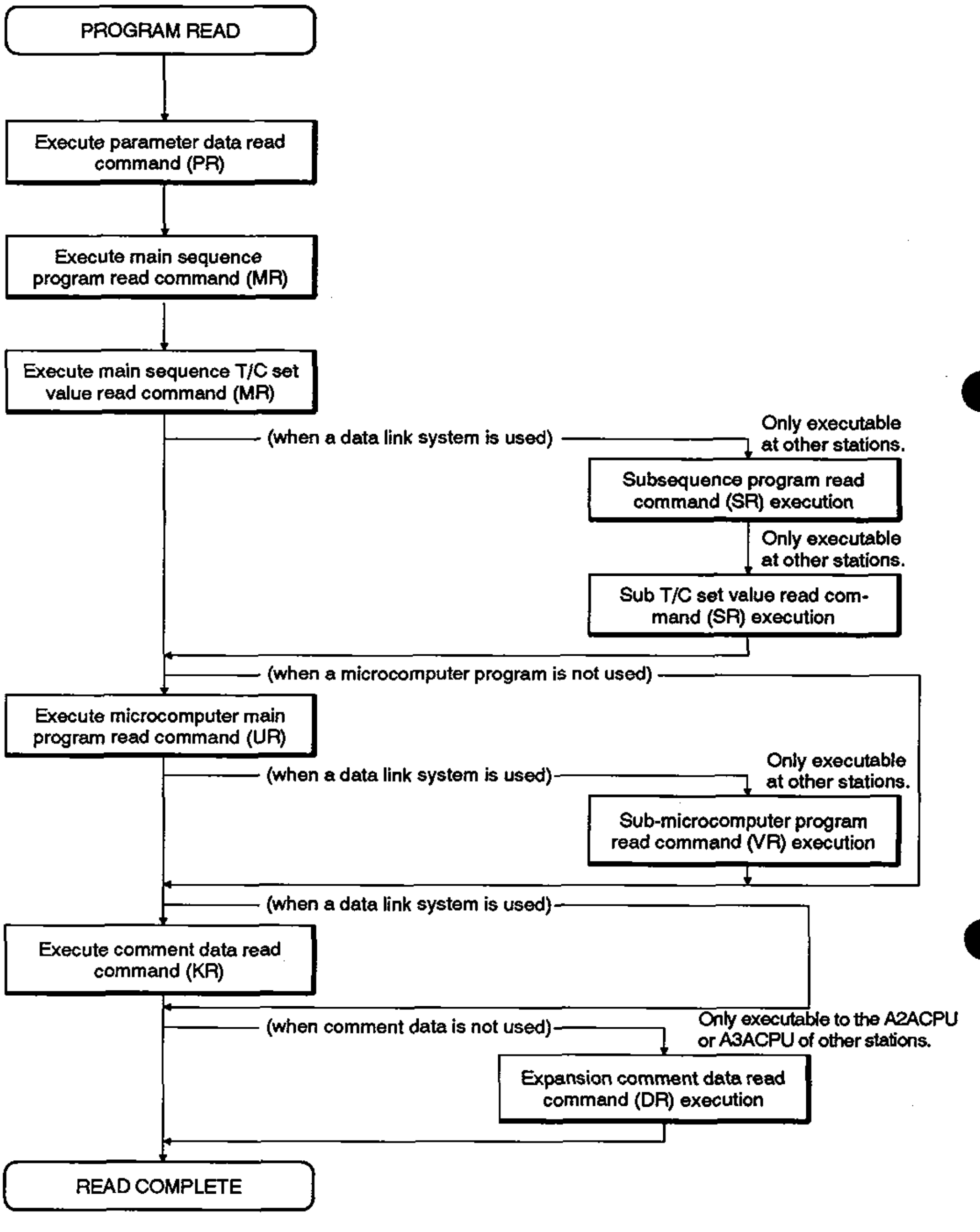
When writing programs, write all stored data to the PC CPU. If all areas have not been written to, the PC CPU will not work correctly.

(2) Before writing programs, write parameter data and execute a parameter analysis request. Otherwise, the parameters in the PC CPU user memory will be changed but the parameters stored in the work area by the ACPU for operation will remain unchanged. Therefore, if a peripheral device is loaded and operated after the parameters are changed, processing will be carried out with the previous parameters, which are still stored in the work area.

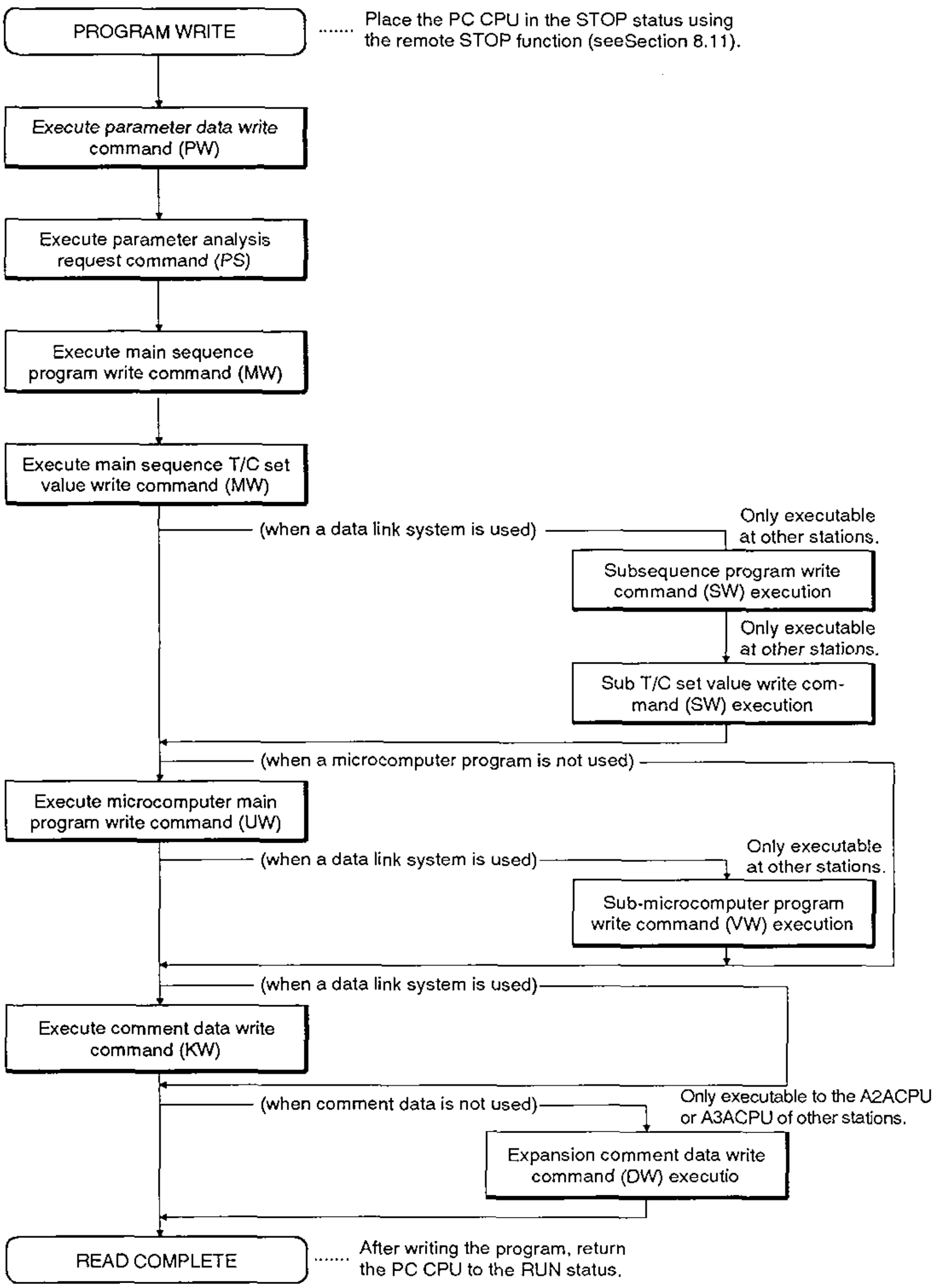
(3) The number of points which can be processed per communications is fixed. When reading or writing data, divide the data into several groups to read or write the entire area. Parameter data should be divided into 3K bytes. Other data shoule be divided into units of data determined by parameter setting.

8.12.2 Program read/write control procedures

(1) Reading



(2) Writing


PROGRAM WRITE
.... Place the PC CPU in the STOP status using the remote STOP function (seeSection 8.11).
Execute parameter data write command (PW)
Execute parameter analysis request command (PS)
Execute main sequence program write command (MW)
Execute main sequence T/C set value write command (MW)
(when a data link system is used)
Only executable at other stations.
Subsequence program write command (SW) execution
Only executable at other stations.
Sub T/C set value write com-mand (SW) execution
(when a microcomputer program is not used)
Execute microcomputer main program write command (UW)
(when a data link system is used)
Only executable at other stations.
Sub-microcomputer program write command (VW) execution
(when a data link system is used)
Execute comment data write command (KW)
(when comment data is not used)
Only executable to the A2ACPU or A3ACPU of other stations.
Expansion comment data write command (DW) executio
READ COMPLETE
.... After writing the program, return the PC CPU to the RUN status.

8.12.3 Parameter memory read/write

(1) Commands and addresses

(a) ACPU common commands

Item	Command		Processing	Number of Points Processed per Communication	PC CPU State			Access to A1SCPU	Access to PC CPU in Data Link
	Symbol	ASCII code			During STOP	During RUN			
						SW04 ON	SW04 OFF		
Batch read	PR	50H, 52H	Reads parameters.	128 bytes	o	o	o	o	o
Batch write	PW	50H, 57H	Writes parameters.		o	x	x	o	o
Analysis request	PS	50H, 53H	Causes the PC CPU to acknowledge and check rewritten parameters.		o	x	x	o	o

Note : o .... Executable
x .... Unavailable

(b) Parameter addresses

There are 3K bytes of parameter memory, addresses 00000H to 00BFFH. For addresses, use 5-digit ASCII (hexadecimal).

POINT

After changing parameters, always call the parameter analysis request command (PS).

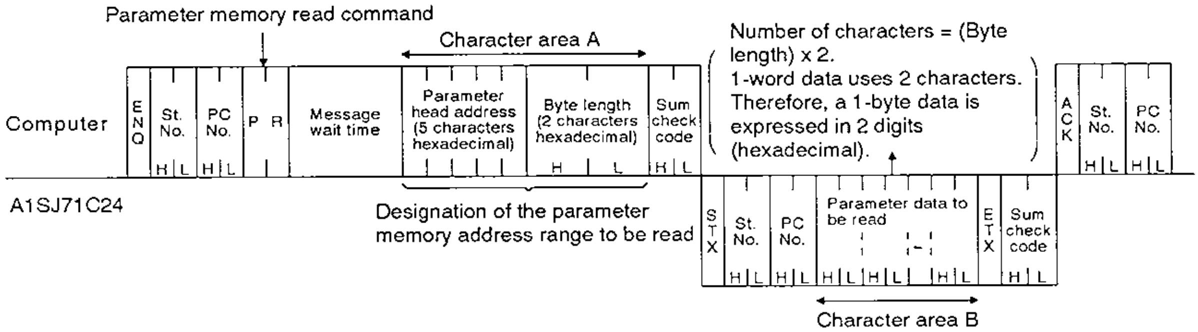
If this is not done, the parameters in PC CPU user memory will be changed but the parameters stored in the work area by the ACPU for operation will remain unchanged. Therefore, if a peripheral device is loaded and operated after the parameters are changed, processing will be executed with the previous parameters, which are still stored in the work area.

(2) Parameter memory batch read (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



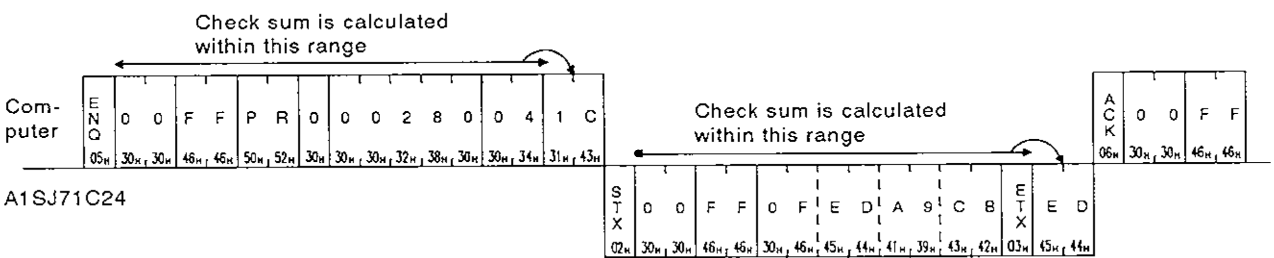
POINT

To designate the byte length, the following condition must be met:

- 1 ≤ byte length ≤ 128

Designation Example

To read 4-byte parameter data in parameter memory addresses 280H to 283H of the A1SCPU. (Message wait time is 0 msec)



Indicates that:

The contents of parameter memory address 280H is 0FH

The contents of parameter memory address 281H is EDH

The contents of parameter memory address 282H is A9H

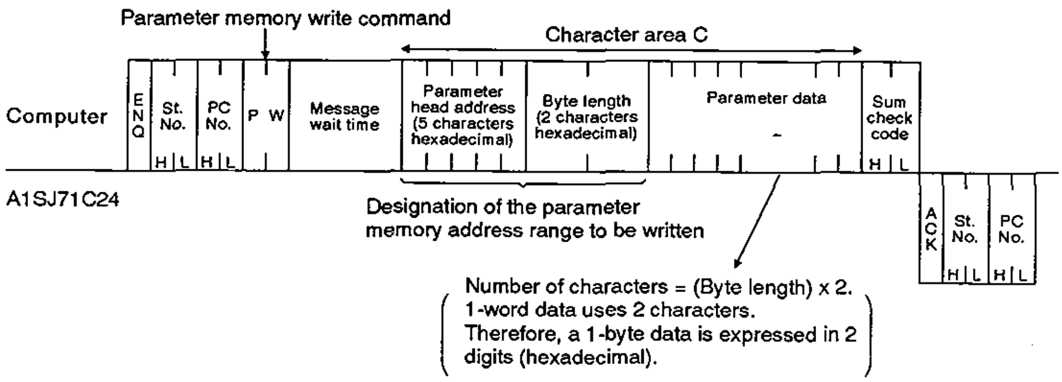
The contents of parameter memory address 283H is CBH

(3) Parameter memory batch write (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



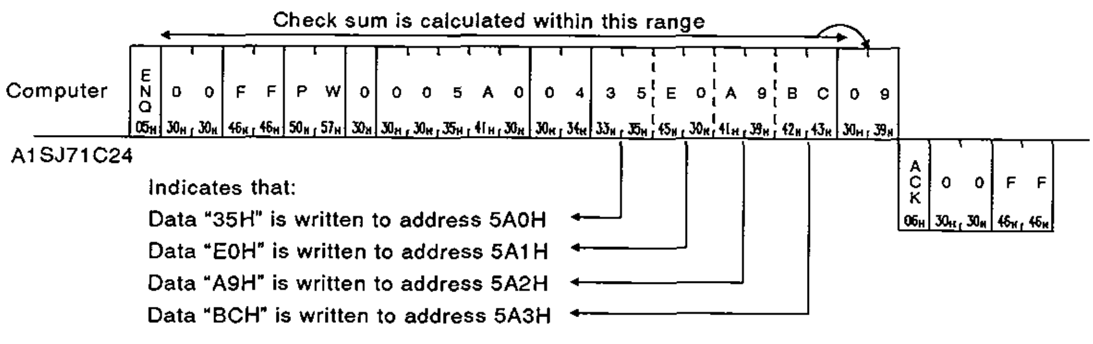
POINT

To designate the byte length, the following condition must be met:

- 1 ≤ byte length ≤ 128

Designation Example

To write 4-byte data to parameter memory addresses 5A0H to 5A3H of the A1SCPU.
(Message wait time is 0 msec)

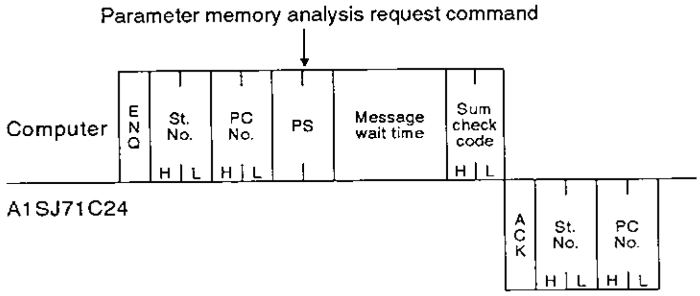


(4) Parameter memory analysis request (ACPU common command)

Designation Method

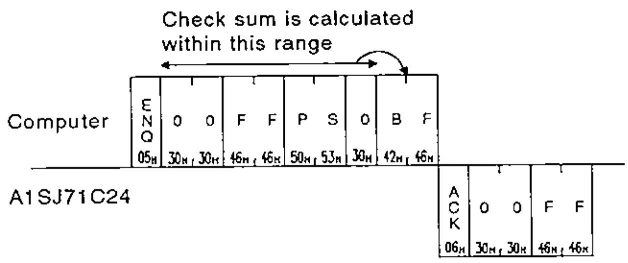
St. No. : Station number

Designation in protocol 1 is shown below.



Designation Example

To request parameter memory analysis after writing parameter to the A1SCPU.
(Message wait time is 0 msec)



8.12.4 Sequence program read/write

(1) Commands and step allocation

(a) ACPU common commands

Item			Command		Processing	Number of Points Processed per Communication	PC CPU State			Access to A1SCPU	Access to PC CPU in Data Link
			Symbol	ASCII Code			During STOP	During RUN SW04 ON	During RUN SW04 OFF		
Batch read	Main	Except T/C set value	MR	4DH, 52H	Reads main sequence program.	64 steps	o	o	o	o	o
		T/C set value			Reads T/C set values used in main sequence programs.	64 points					
	Sub	Except T/C set value	SR	53H, 52H	Reads subsequence program.	64 steps	o	o	o	x	o
		T/C set value			Reads T/C set values used in subsequence programs.	64 points					
Batch write	Main	Except T/C set value	MW	4DH, 57H	Writes main sequence program.	64 steps	o	o*	x	o	o
		T/C set value			Writes T/C set values used in main sequence programs.	64 points	o	o	x		
	Sub	Except T/C set value	SW	53H, 57H	Writes subsequence program.	64 steps	o	o*	x	x	o
		T/C set value			Writes T/C set values used in subsequence programs.	64 points	o	o	x		

Note : o ....Executable
x ....Not executable

* Writing during a program run may be executed if all the following conditions are met:

1) The PC CPU is A3, A3N, A3H, A3M, A73, or A3A.

2) The program is not the currently running program (indicates a subprogram called by the main program, if the main program is being run).

3) The PC CPU special relay is in the following state:

i) M9050 (signal flow conversion contact).....OFF (A3CPU only)

ii) M9051 (CHG instruction disable)...............ON

POINT

When reading or writing the timer/counter setting values using the sequence program read/write command, range designations of T0 to T255 or C0 to C255 are possible.

Extended ranges of T256 to T2047 and C256 to C1023 for AnA CPU should be used for storing the setting values; read or write the set values using the batch read/write command for devices (D, W, R) allocated by parameter setting.

(b) Designating the head address

The division between sequence programs and T/C set values, and their addresses in 4-digit ASCII are shown in the table below.

Example:

To read the set values T0 to T63

Head address = FE00H Command = MR

Sequence Program	Designated Step for Protocol
T0 set value T1 set value to T255 set value	FE00H FE01H to FEFFH
C0 set value C1 set value to C255 set value	FF00H FF01H to FFFFH
Step 0 Step 1 to Step 30718 (30K)	0000H 0001H to 77FEH

Calculation of designated step

Timer : Tm = FE00H + n

Counter : Cm = FF00H + n

where, m = device number

n = hexadecimal value of device number

(c) Meaning of T/C set values

T/C set values are stored as hexadecimal values as shown in the table below.

When rewriting the PC CPU set values from the computer via the A1SJ71C24, designate the set value in 4-digit ASCII.

Example:

Data designated to change T10 setting value K10 to K20......0014H

Data designated to change T11 setting value D30 to D10......800AH

Ladder Example in Program	Setting in Program	Setting in Protocol
K[][][][][] T[][][] K[][][][][] C[][][]	K0 K1 to K9 K10 to K32767	0000H 0001H to 0009H 000AH to 7FFFH
D[][][][] T[][][] D[][][][] C[][][]	D0 D1 D2 to D1023	8000H 8002H 8004H to 87FEH

Calculation of protocol setting value

Km = 0000H + n

Dm = 8000H + 2n

where, m = device number

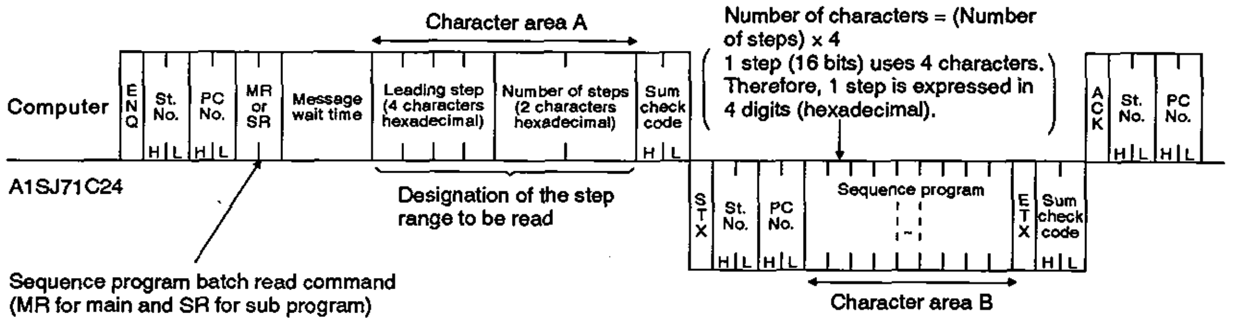
n = hexadecimal value of device number

(2) Sequence program batch read (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



POINTS

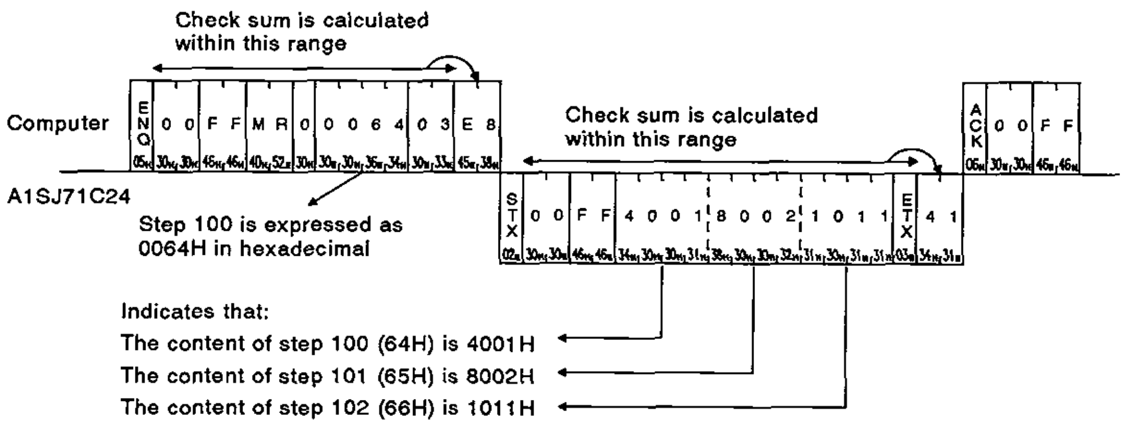
(1) To designate the number of steps, the following condition must be met:

- 1 ≤ number of steps ≤ 64

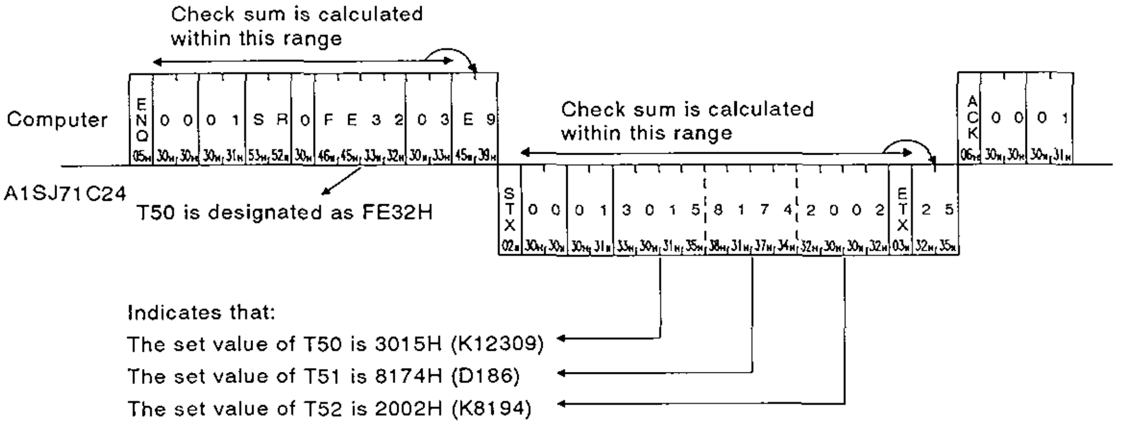
(2) Timers, counters, and a sequence program cannot be used in combination. Only one of these may be set.

Designation Examples

Example 1:
To read 3 steps: step 100 to step 102 of the main sequence program of the A1SCPU.
(Message wait time is 0 msec)



Example 2:
To read set values at 3 points: T50 to T52 of the subsequence program of the A1SCPU.
(Message wait time is 0 msec)

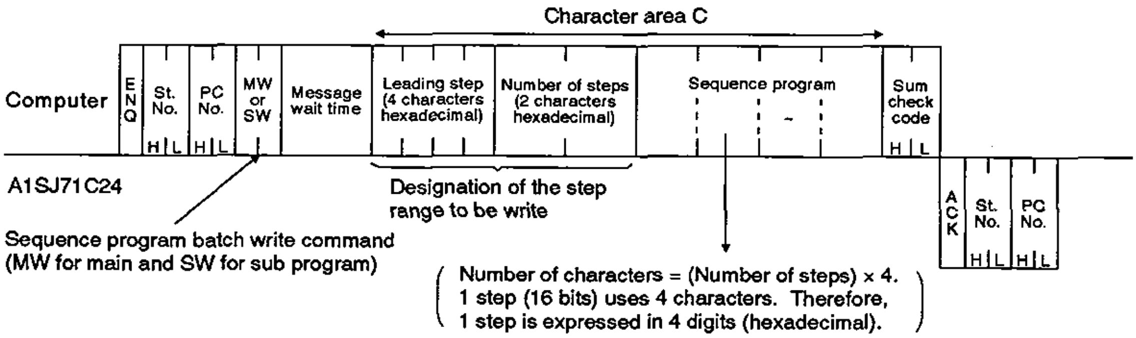


(3) Sequence program batch write (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



POINTS

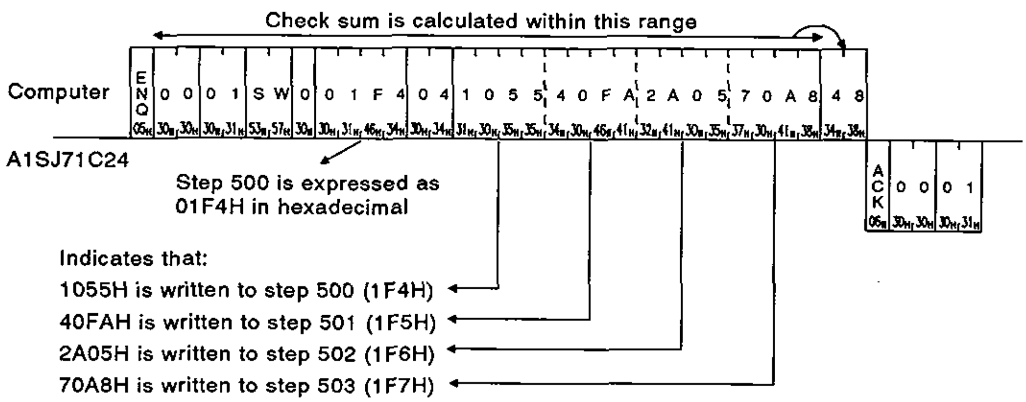
(1) To designate the number of steps, the following condition must be met:

- 1 ≤ number of steps ≤ 64

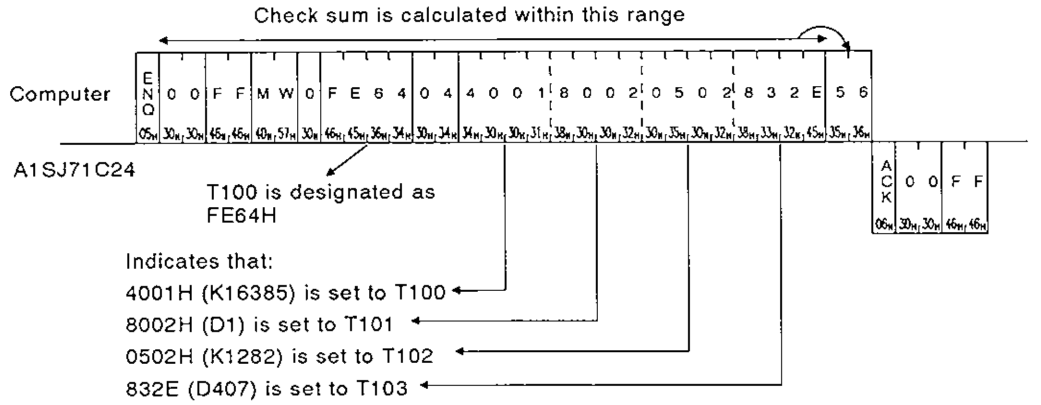
(2) Timers, counters, and the sequence program cannot be used in combination. Only one of these may be set.

Designation Examples

Example 1:
To write a program to 4 steps: step 500 to step 503 of the subsequence program of the A1SCPU. (Message wait time is 0 msec)



Example 2:
To write set values to 4 points: T100 to T103 of the main sequence program of the A1SCPU.
(Message wait time is 0 msec)



8.12.5 Microcomputer program read/write

(1) Commands and addresses

Commands and program addresses to read and write microcomputer programs are explained below:

(a) ACPU common commands

Item		Command Symbol	Command ASCII Code	Processing	Number of Points Processed per Communication	State of PC CPU During STOP	State of PC CPU During RUN SW04 ON	State of PC CPU During RUN SW04 OFF	Access to A1S CPU	Access to PC CPU in Data Link
Batch read	Main	UR	55H, 52H	Reads microcomputer main programs.	128 bytes	o	o	o	o	o
	Sub	VR	56H, 52H	Reads microcomputer subprograms.					x	o
Batch write	Main	UW	55H, 57H	Writes microcomputer main programs.	128 bytes	o	o*	x	o	o
	Sub	VW	56H, 57H	Writes microcomputer subprograms.					x	o

Note : o....... Executable
x....... Not executable

* Writing during a program run may be executed if all the following conditions are met:

1) The PC CPU is A3, A3N, A3H, A3M or A73.

2) The program is not currently running program (indicates a subprogram called by the main program, if the main program is being run).

3) The PC CPU special relay is in the following state:

M9050 (signal flow conversion contact) : OFF (A3CPU only)

M9051 (CHG instruction disable) : ON

(b) Microcomputer program address

Microcomputer addresses are designated in the protocol as follows:

1) The range of addresses that can be set for each PC CPU is shown in the table on the next page.

CPU Model	Microcomputer Program Capacity	Microcomputer Program Addresses
A1SCPU A0J2HCPU A2CCPU	Max. 14K bytes	0000H to 37FEH
A1CPU A1NCPU	Max. 10K bytes	0000H to 27FEH
A2CPU(S1) A2NCPU(S1)	Max. 26K bytes	0000H to 67FEH
A3CPU A3NCPU A3HCPU A3MCPU A73CPU	Main and sub Max. 58K bytes	0000H to E7FEH

2) Addresses are set by converting 4-digit hexadecimals into ASCII.

3) A character area error 06H occurs if the following condition is not met:

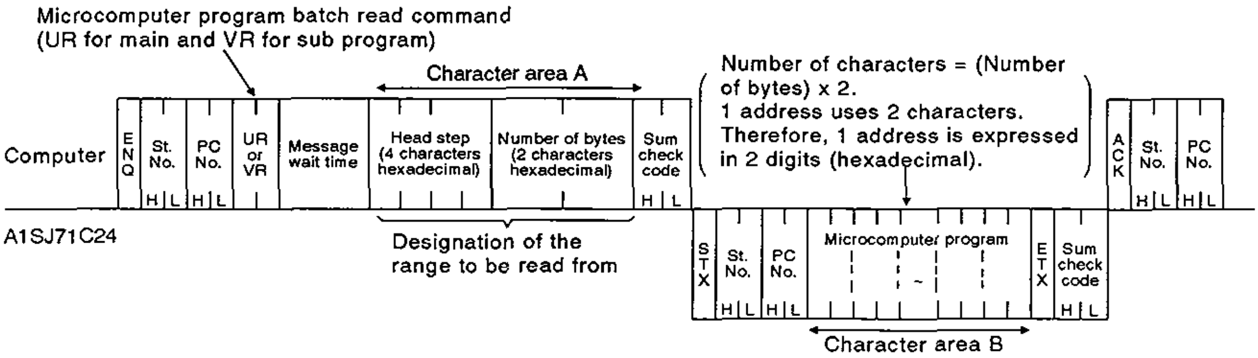
   Head address + (number of bytes) – 1 ≥ microcomputer program capacity.

(2) Microcomputer program batch read (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



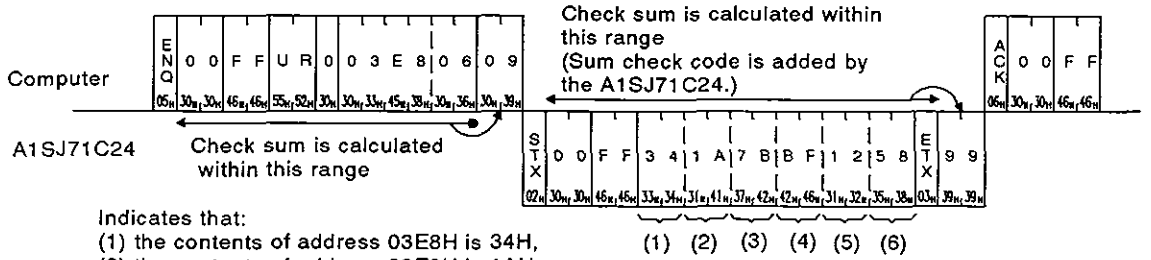
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + [(number of bytes) – 1] ≤microcomputer program capacity

Designation Example

To read 6 bytes of a microcomputer program beginning with address 03E8H (1000 in decimal) in the A1SCPU. (Message wait time is 0 msec)



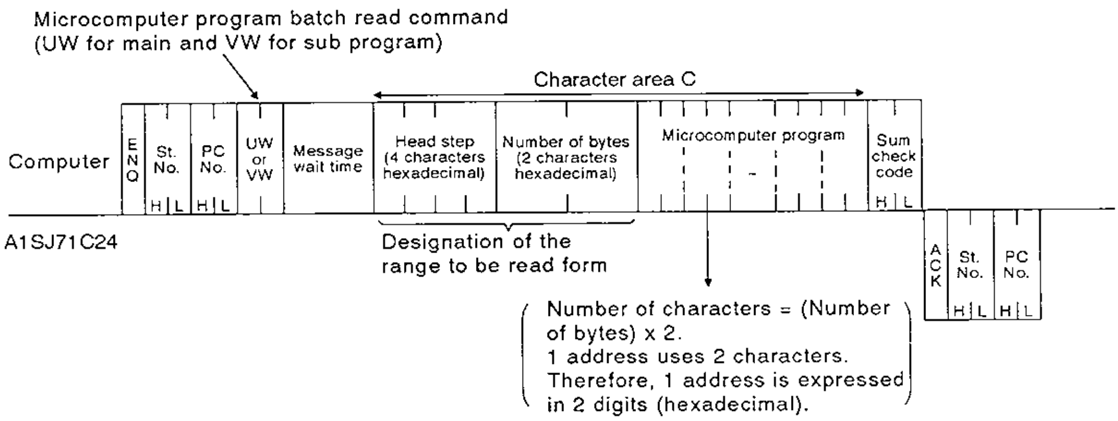
Indicates that:
(1) the contents of address 03E8H is 34H,
(2) the contents of address 03E9H is 1AH,
(3) the contents of address 03EAH is 7BH,
(4) the contents of address 03EBH is BFH,
(5) the contents of address 03ECH is 12H, and
(6) the contents of address 03EDH is 58H.

(3) Microcomputer program batch write (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



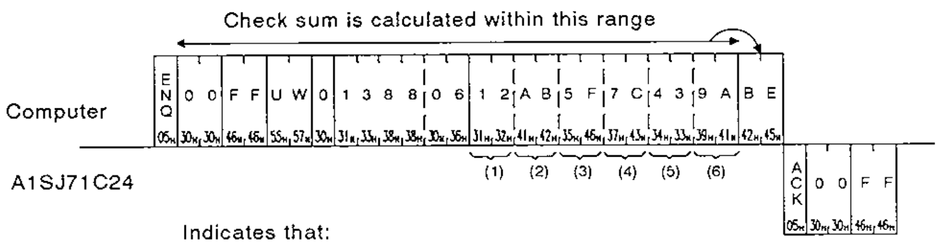
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + (number of bytes) – 1 ≤ Microcomputer program capacity

Designation Example

To write 6 bytes of a microcomputer program to the area beginning with address 1338H (5000 in decimal) in the A1SCPU. (Message wait time is 0 msec)



Indicates that:
(1) 12H is written to address 1388H,
(2) ABH is written to address 1389H,
(3) 5FH is written to address 138AH,
(4) 7CH is written to address 138BH,
(5) 43H is written to address 138CH, and
(6) 9AH is written to address 138DH.

8.12.6 Comment memory read/write

(1) Commands and addresses

Commands and comment data addresses to read and write comment data are explained below.

(a) ACPU common commands

Item		Command		Processing	Number of Points Processed per Communication	State of PC CPU			Access to A1S CPU	Access to PC CPU in Data Link
		Symbol	ASCII Code			During STOP	During RUN			
							SW04 ON	SW04 OFF		
Batch read	Main	KR	4BH, 52H	Reads from comment memory.	128 bytes	o	o	o	o	o
Batch write	Sub	KW	4BH, 57H	Writes to comment memory.	128 bytes	o	o	x	o	o

Note : o....... Executable
x....... Not executable

(b) Comment memory addresses

The area to store comment data is managed using relative addresses from the head address 00H.

For example, for 2K bytes of parameter comments, the range in which the addresses may be specified for the head address is 00H to 7FFH.

1) Comment memory capacity is 64K bytes

The comment data address range is determined by the parameter setting.

2) Comment memory addresses are designated in 4-digit ASCII. (0000 to FFFF)

3) A character area error 06H occurs if the following condition is not met:

Head address + designated number of bytes –1 ≤ comment memory capacity.

POINT

It is not possible to designate a particular device or device number when reading or writing comment data.

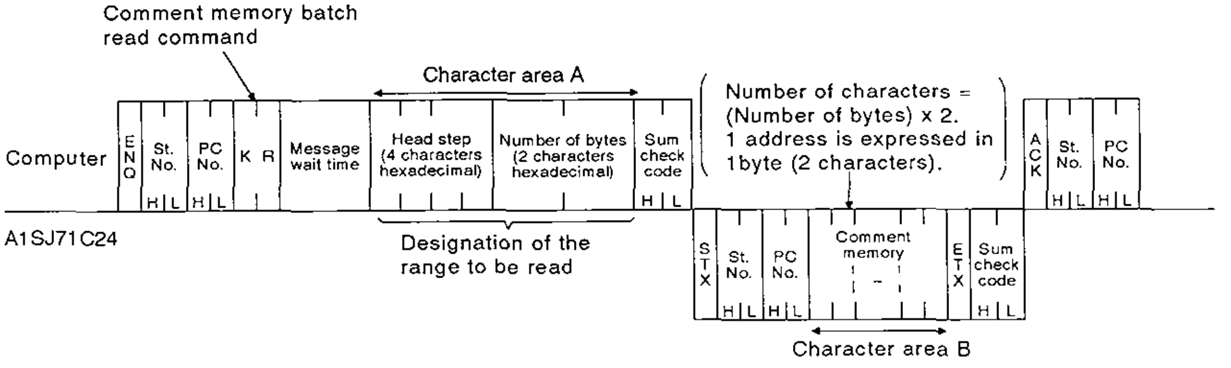
Always read or write all data from address 0H.

(2) Comment memory batch read (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



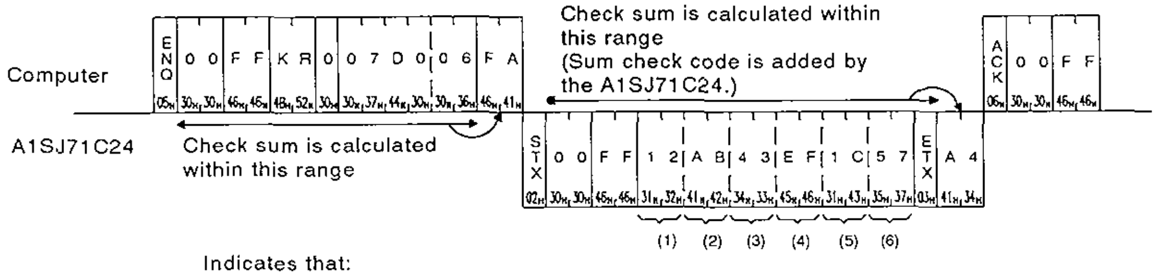
POINT

To designate the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + (number of bytes) − 1 ≤ Comment memory capacity

Designation Example

To read 6 bytes of comment memory data beginning with address 7D0H (2000 in decimal) in the A1SCPU. (Message wait time is 0 msec)



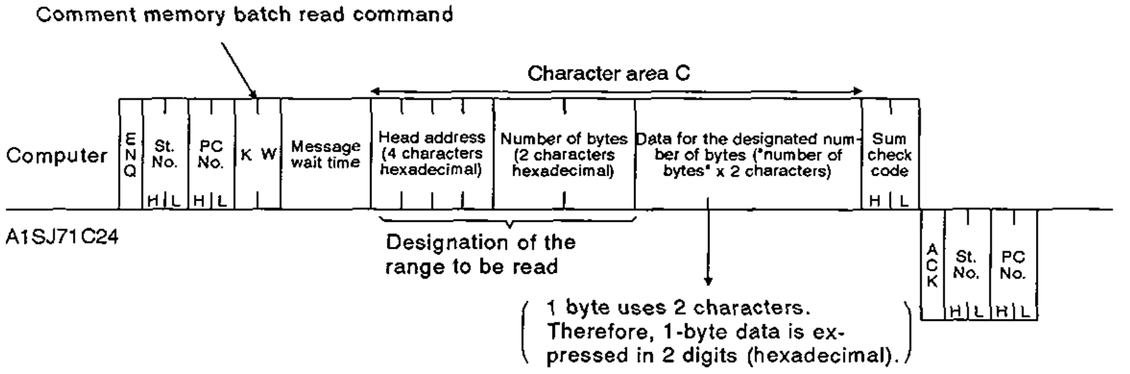
Indicates that:
(1) the content of address 07D0H is 12H,
(2) the content of address 07D1H is ABH,
(3) the content of address 07D2H is 43H,
(4) the content of address 07D3H is EFH,
(5) the content of address 07D4H is 1CH, and
(6) the content of address 07D5H is 57H.

(3) Comment memory batch write (ACPU common command)

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



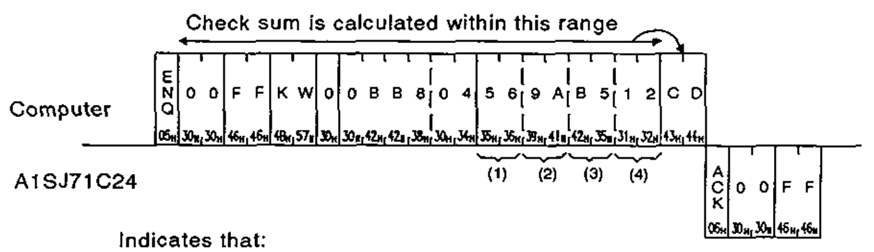
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + (number of bytes) − 1 ≤ Comment memory capacity

Designation Example

To write 4 bytes of comments to the area beginning with address 0BB8H (3000 in decimal) in the A1SCPU. (Message wait time is 0 msec)



Indicates that:
(1) 56H is written to address 0BB8H,
(2) 9AH is written to address 0BB9H,
(3) B5H is written to address 0BBAH, and
(4) 12H is written to address 0BBBH.

8.12.7 Extension comment memory read/write

(1) Commands and addresses

(a) AnACPU dedicated commands

Item	Command		Processing	Number of Point Processed per Communication	State of PC CPU			Access to A1S CPU	Access to PC CPU in Data Link
	Symbol	ASCII Code			During STOP	During RUN			
						SW04 ON	SW04 OFF		
Batch read	DR	44H, 52H	Reads from the extension comment memory.	128 bytes	o	o	o	x	o
Batch write	DW	44H, 57H	Writes to the extension comment memory.	128 bytes	o	o	x	x	o

Note : o .... Executable
x .... Not executable

(b) Extension comment memory addresses

The extension comment data storage area is managed in relative addresses with the head address 00H.

For example, the range that can be set to the head address for an extension comment memory of 3K bytes is 00H to BFFH.

1) The maximum extension comment memory area is 64K bytes.

The address range for the extension comment data is determined in accordance with the paraemter set capacity.

2) Designation of the extension comment memory address is made by converting 5-digit hexadecimal into ASCII code (00000 to 0FBFF).

3) A character error "06H" occurs if the extension comment memory capacity is not equal to or greater than [head address + (set number of bytes – 1)].

POINT

Reading or writing extension comment data by designating specific devices or device numbers is not possible.

Always read or write extension comment data beginning with address 0H.

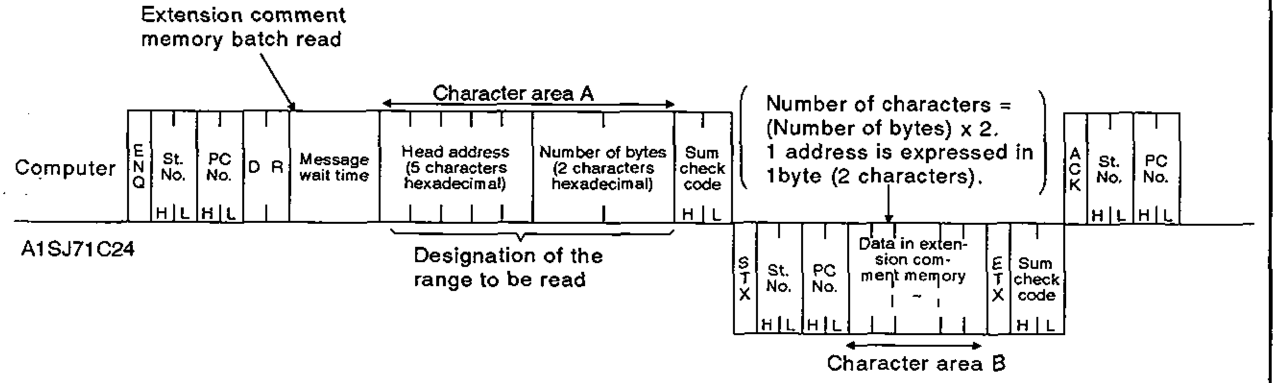
(2) Extension comment memory batch read

Batch read of the extension comment memory using an AnACPU dedicated command is shown below.

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



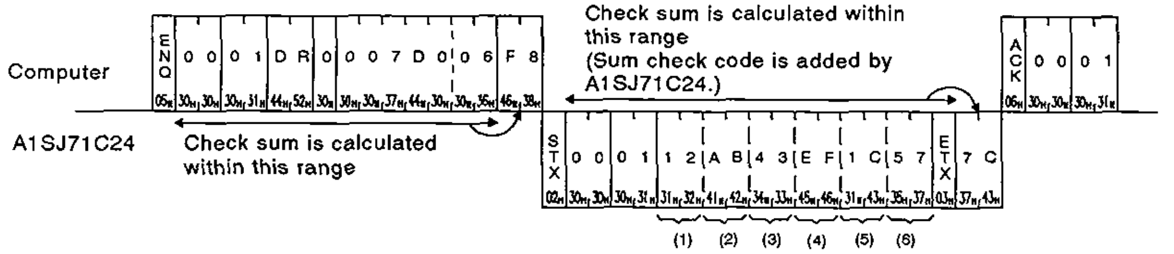
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + (number of bytes) − 1 ≤ extension coment memory capacity

Designation Example

To read 6 bytes of data from the extension comment memory beginning with 7D0H (2000 in decimal) in PC number "1". (Message wait time is 0 msec)



Indicates that:
(1) the content of address 07D0H is 12H,
(2) the content of address 07D1H is ABH,
(3) the content of address 07D2H is 43H,
(4) the content of address 07D3H is EFH,
(5) the content of address 07D4H is 1CH, and
(6) the content of address 07D5H is 57H.

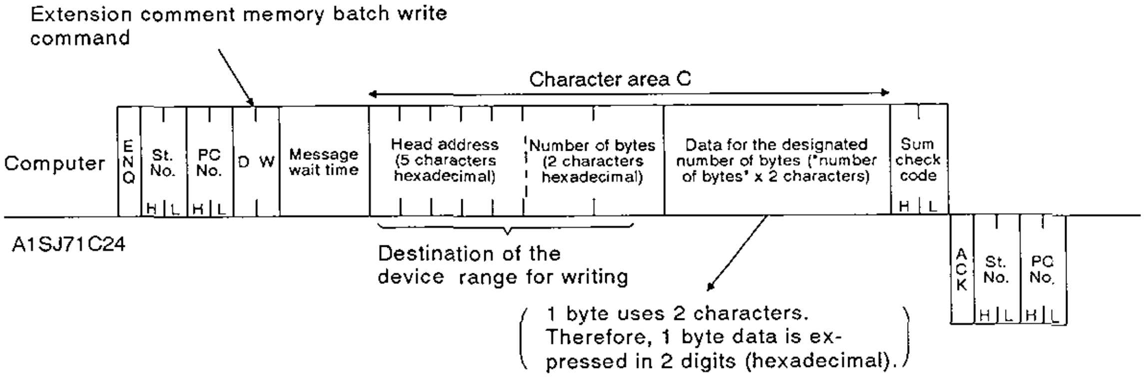
(3) Extension comment memory batch write

Batch write of data to the extension comment memory using an AnACPU dedicated command is shown below.

Designation Method

St. No. : Station number

Designation in protocol 1 is shown below.



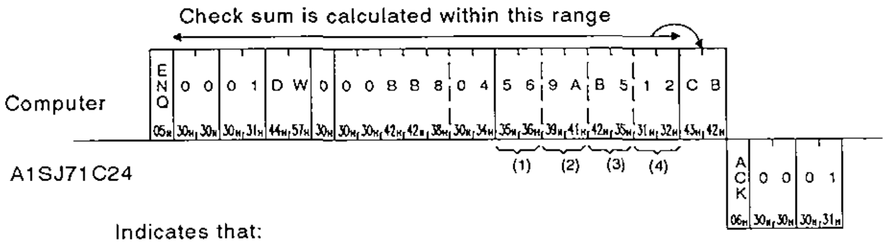
POINT

To set the number of bytes, the following conditions must be met:

- 1 ≤ number of bytes ≤ 128
- (Head address) + (number of bytes) − 1 ≤ extension comment memory capacity

Designation Example

To write 4 bytes of extension comment to the extension comment memory area beginning with 0BB8H (3000 in decimal) in PC number "0". (Message wait time is 0 msec)



Indicates that:
(1) 56H is written to address 0BB8H,
(2) 9AH is written to address 0BB9H,
(3) B5H is written to address 0BBAH, and
(4) 12H is written to address 0BBBH.

8.13 Global Function

The global function is used to switch the Xn2 input signal at each A1SJ71C24 in all stations connected to the computer by the multidrop link.

This function is used for emergency instructions simultaneous start, etc., to the A1SCPU.

8.13.1 Commands and control

(1) ACPU common commands

Item	Command		Processing	State of PC CPU			Access to A1S CPU	Access to PC CPU in Data Link
	Symbol	ASCII Code		During STOP	During RUN			
					SW04 ON	SW04 OFF		
Global	GW	47H, 57H	Turns ON/OFF Xn2 of the AJ71C24 loaded in each PC CPU system.	o	o	o	o	x

Note : o....... Executable

(2) Control

This function switches the Xn2 input signal at each A1SJ71C24 in all stations linked to the computer.

(a) Xn2 is determined by the I/O addresses of the A1SJ71C24s.

Example: If the I/O addresses are 90 to AF, Xn2 is X92.

(b) Designate the station number in the control protocol as 00H.

Designating a number other than 00H causes the Xn2 of the A1SJ71C24 at the designated station number to turn ON/OFF.

(c) This function is a command from the computer. A reply is not given by the A1SJ71C24.

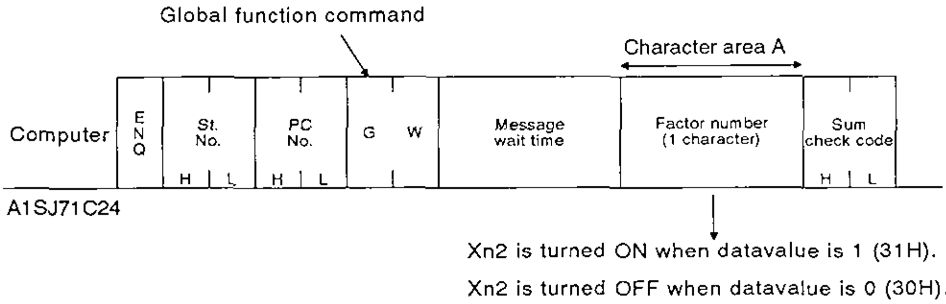
(d) Xn2 is cleared from any station when the power supply to the station is turned OFF or when the CPU or the station is reset.

8.13.2 Setting the global function (ACPU common command)

Designation Method

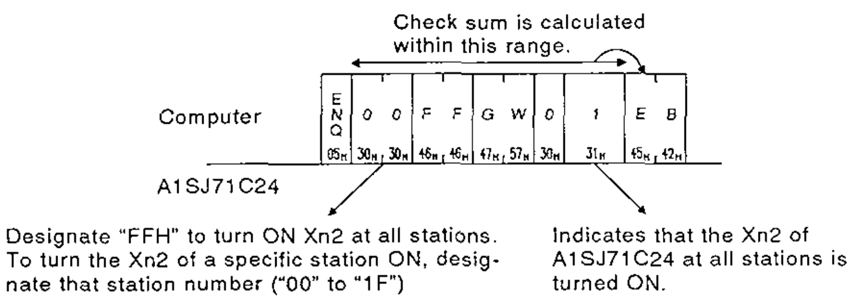
St. No. : Station Number

Designation in protocol 1 is shown below.



Designation Example

To turn the Xn2 of A1SJ71C24 ON. (Message wait time is 0 msec.)

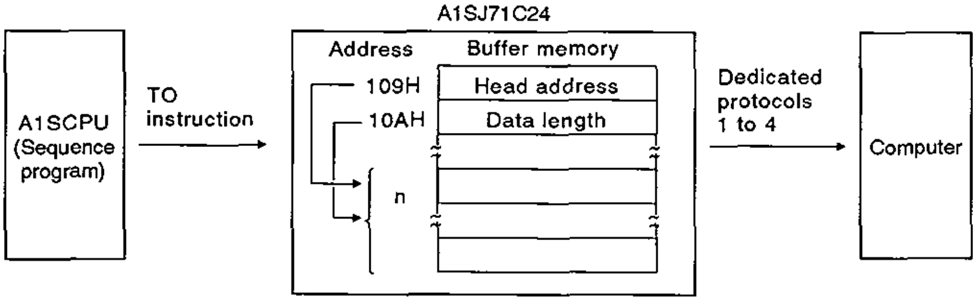


8.14 On-demand Function

The on-demand function is used when the A1SCPU has data to transmit to the computer. In this case, the A1SCPU specifies the buffer memory area in which the data to be transmitted is stored and then starts transmission.

During data transmission between the computer and A1SCPU using dedicated protocols 1 to 4, communications is normally initiated by the computer.

If the A1SCPU has emergency data to transmit to the computer, the on-demand function is used.



8.14.1 On-demand handshake signal and buffer memory

(1) On-demand handshake signal

The on-demand handshake signal turns ON when the A1SCPU transmits a data send request to the computer to start transmission, and turns OFF when transmission of the data specified by the A1SJ71C24 is completed. It acts as an interlock to prevent on-demand requests being made simultaneously.

Handshake Signal	Description	Signal Turned ON/OFF by
Xn3*	During execution of on-demand function ON : transmission underway OFF : transmission completed	A1SJ71C24

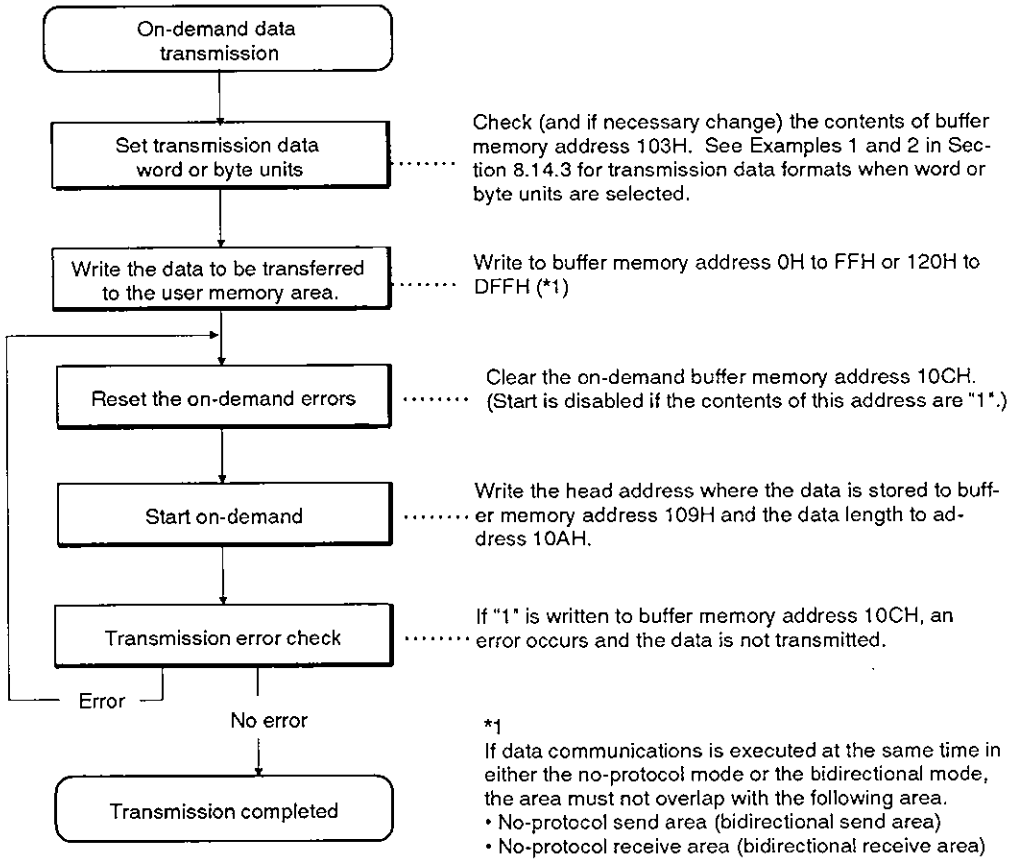
* "n" in Xn3 is determined by the slot location of the A1SJ71C24.

(2) Buffer memory used by the on-demand function

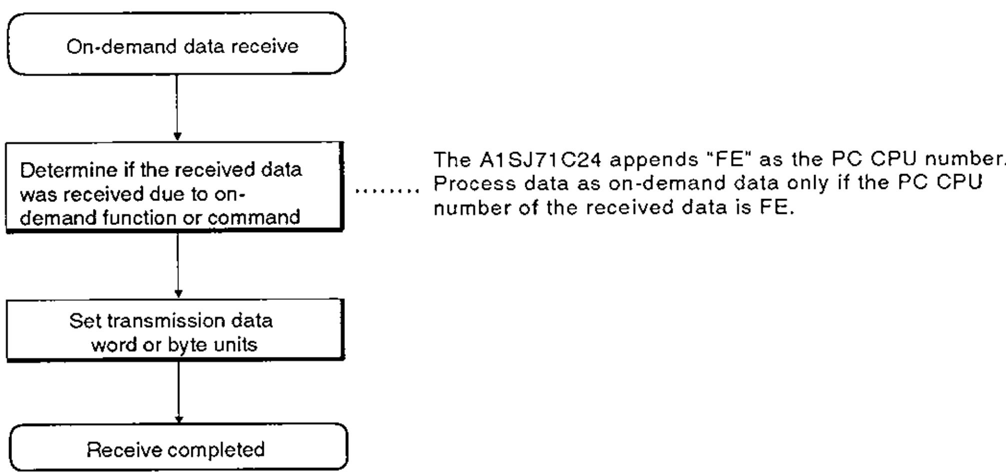
Address	Name	Description
109H	Area to specify head address in on-demand buffer memory	The head address of the data stored in the buffer memory to be transmitted by the on-demand function is specified by the TO instruction of the Sequence program.
10AH	Area to specify data length	The length of the data to be transmitted by the on-demand function is specified by the A1SCPU TO instruction of the sequence program.
10CH	On-demand error storage area	The A1SJ71C24 writes a "1" to this address if a transmission error occurs during on-demand data transmission. 0 : No error 1 : Error

8.14.2 On-Demand function control procedure

(1) A1SCPU control procedure



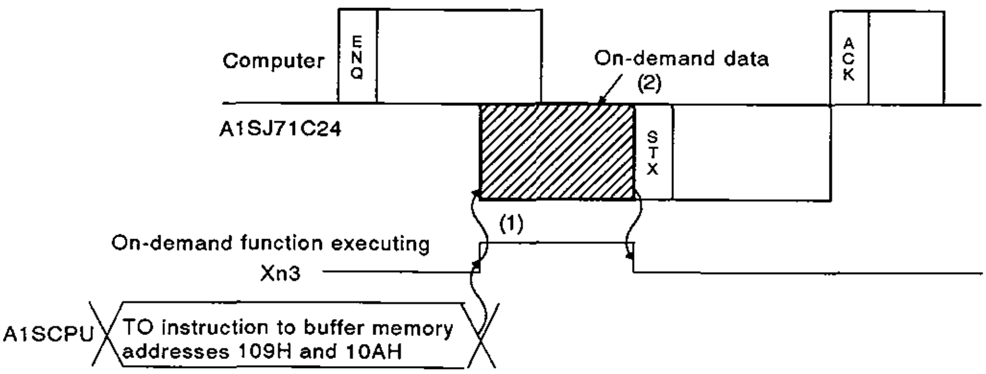
(2) Computer control procedure



(3) On-demand request processing timing chart

(a) Full-duplex communications

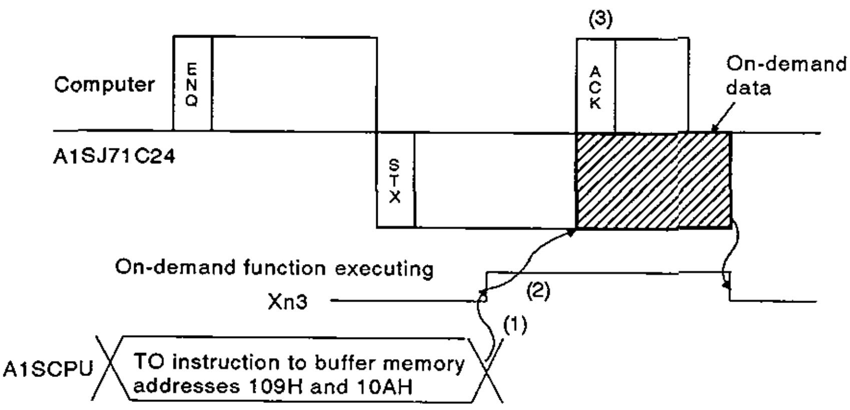
Computer is transmitting data



1) The on-demand function executing signal (Xn3) turns ON immediately and , the on-demand data is transmitted when the on-demand request is made.

2) Transmission of response data (beginning with STX) to the command data (beginning with ENQ) is suspended until the completion of on-demand data transmission.

Computer is receiving data



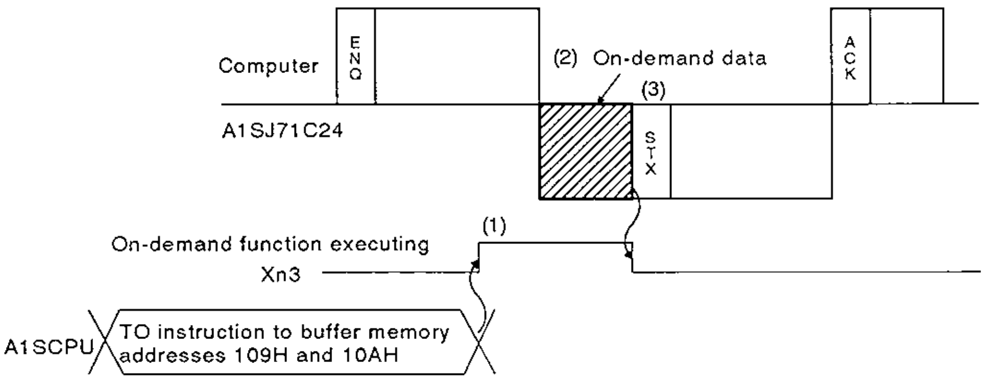
1) The on-demand function executing signal (Xn3) turns ON immediately when the on-demand request is made.

2) Transmission of the on-demand data is suspended until the completion of the response data (beginning with STX) to the command data (beginning with ENQ).

3) Transmission of the response data (beginning with ACK) from the computer in response to the response data (beginning with STX) from the A1SJ71C24 is possible while the on-demand data is received.

(b) Half-duplex communications

Computer is transmitting data

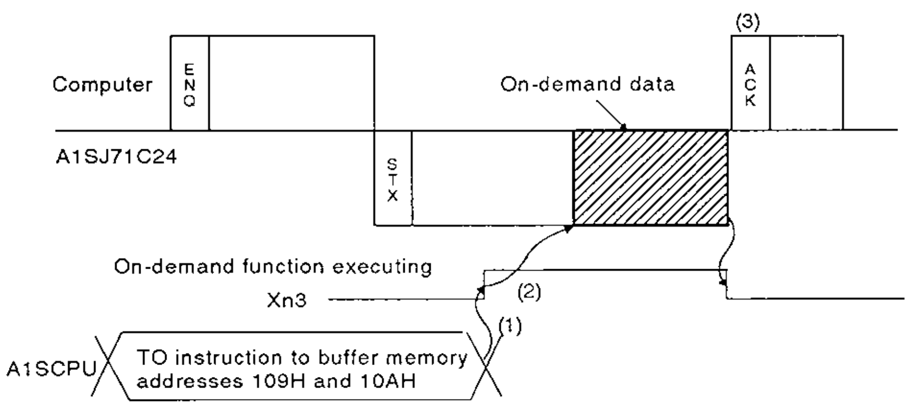


1) The on-demand function executing signal (Xn3) turns on immediately when the on-demand request is made.

2) Transmission of on-demand data is suspended until the completion of command data receive (beginning with ENQ) from the computer.

3) Transmission of response data (beginning with STX) to the command data (beginning with ENQ) is suspended until the completion of on-demand data transmission.

Computer is receiving data



1) The on-demand function executing signal (Xn3) turns ON immediately when the on-demand request is made.

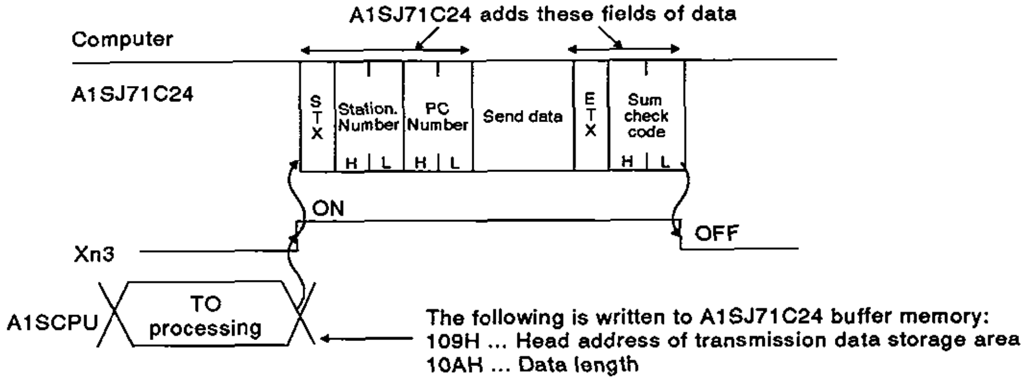
2) Transmission of the on-demand data is suspended unil the completion of the response data (beginning with STX) to the command data (beginning with ENQ).

3) Transmission of the response data (beginning with ACK) from the computer in response to the response data (beginning with STX) from the A1SJ71C24 should be made after the completion of on-demand data receive.

8.14.3 On-demand function designation

Designation Method

Designation in protocol 1 is shown below.



POINTS

(1) Buffer memory area 100H to 11FH is the special applications area.

Do not use this area to store the data to be transmitted with the on-demand function.

(2) Data length setting range must meet the following criteria:

- When the buffer memory area of 0H to FFH is used:

  (Head address) + (data length) − 1 ≤ FFH

- When the buffer memory area of 120H to 7FFH is used:

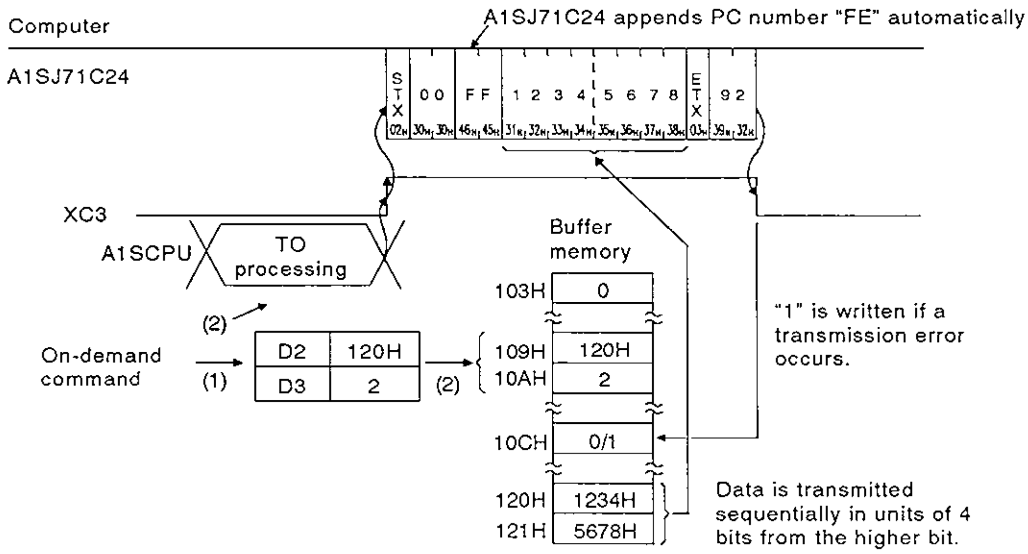
  (Head address) + (data length) − 1 ≤ 7FFH

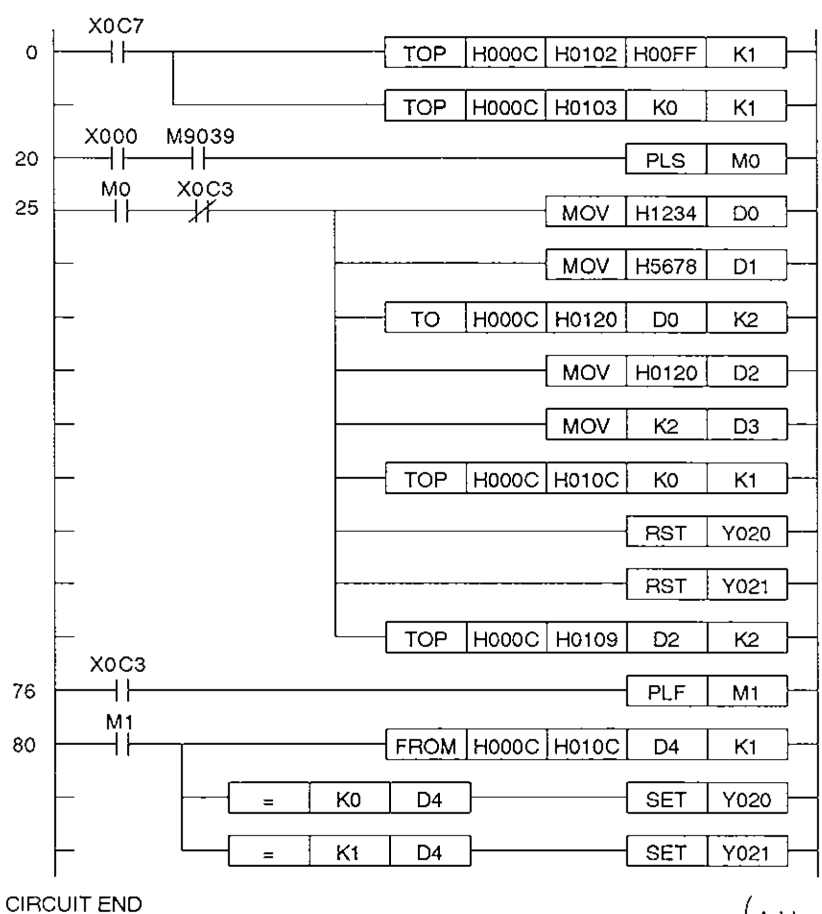
(3) The A1SJ71C24 appends "FE" as the PC CPU number.

(4) The block number is "00H" when protocol 2 is used.

Designation Examples

Example 1:
To start transmission of data, stored in buffer memory at addresses 120H and 121H, by the sequence program. (A1SJ71C24 I/O addresses are C0 to DF,transmission data is designated in word units.)





Request to turn OFF error indicator LED

Sets word unit for data transmission

Converts the start signal to PLS

Sets transmission data

(1) Designates head address of the transmission data storage area and data length

Resets the on-demand error

(Start is disabled if the content at address 10CH is "1".)

(2) Starts the on-demand function

Transmission completed flag

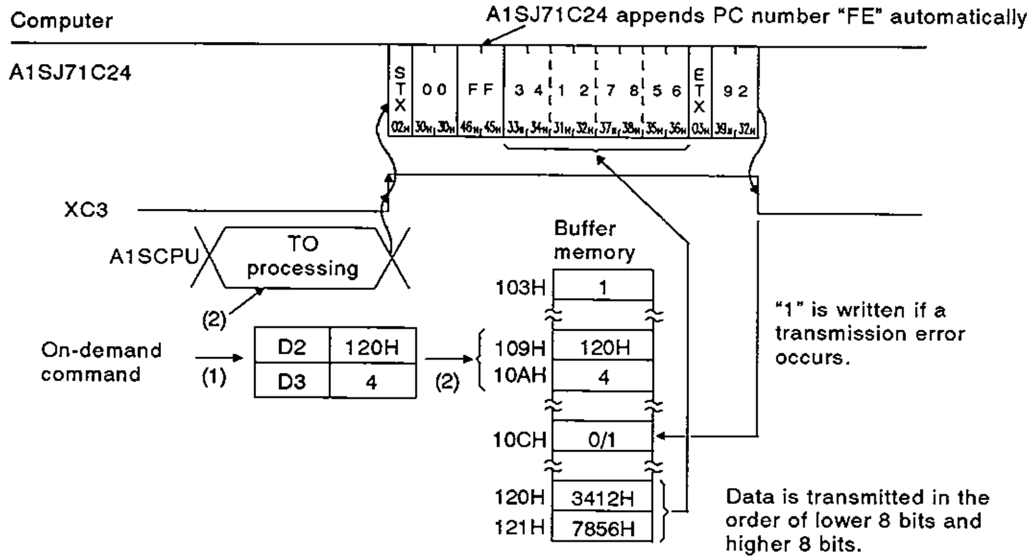
Reads the transmission error storage area to check transmission status

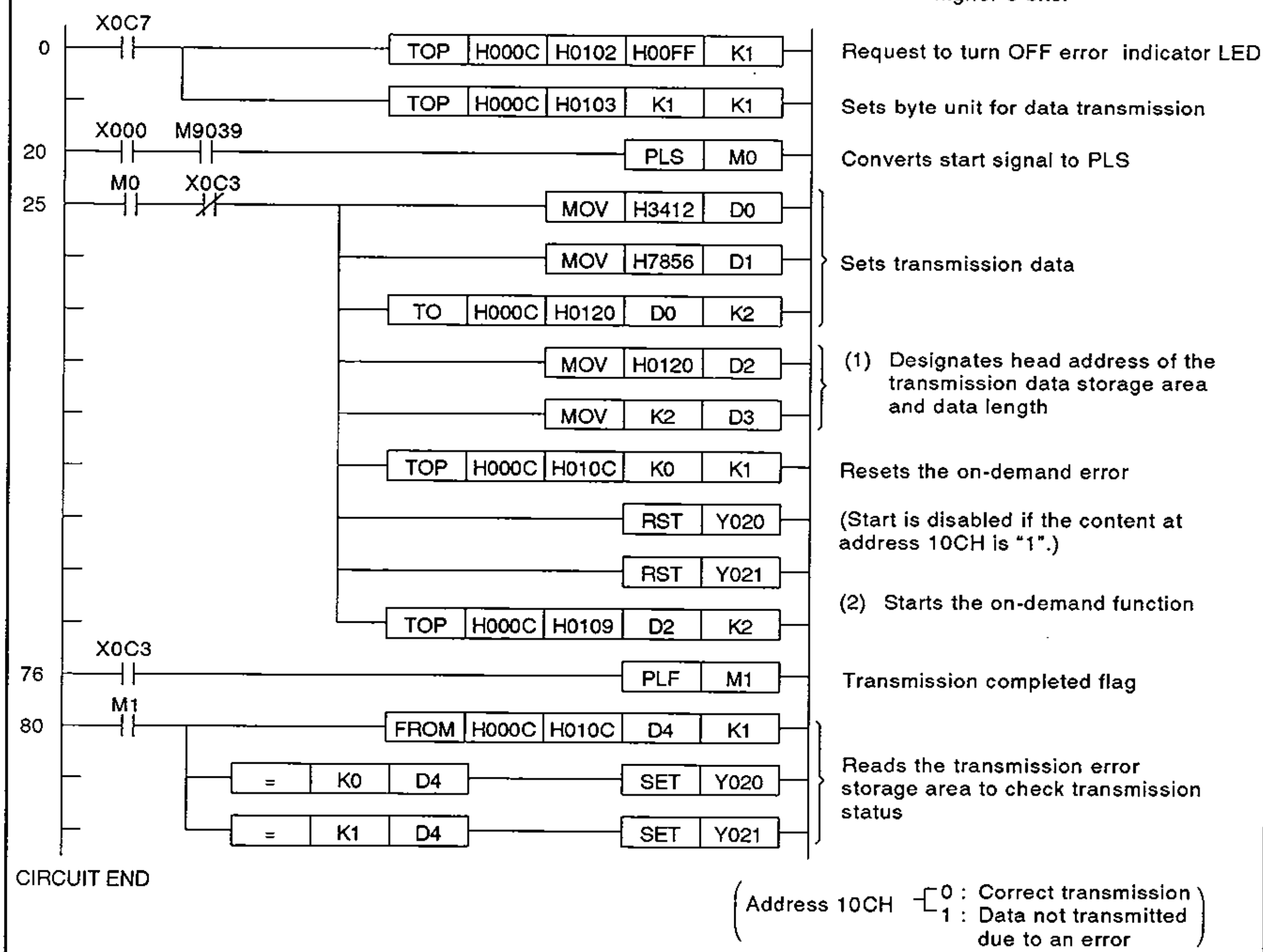
(Address 10CH — 0 : Correct transmission; 1 : Data not transmitted due to an error)

Designation Examples

Example 2:

To start transmission of data, stored in buffer memory at addresses 120H and 121H, by the sequence program. (A1SJ71C24 I/O addresses are 80 to 9F,transmission data is designated in byte units.)





8.15 Loopback Test

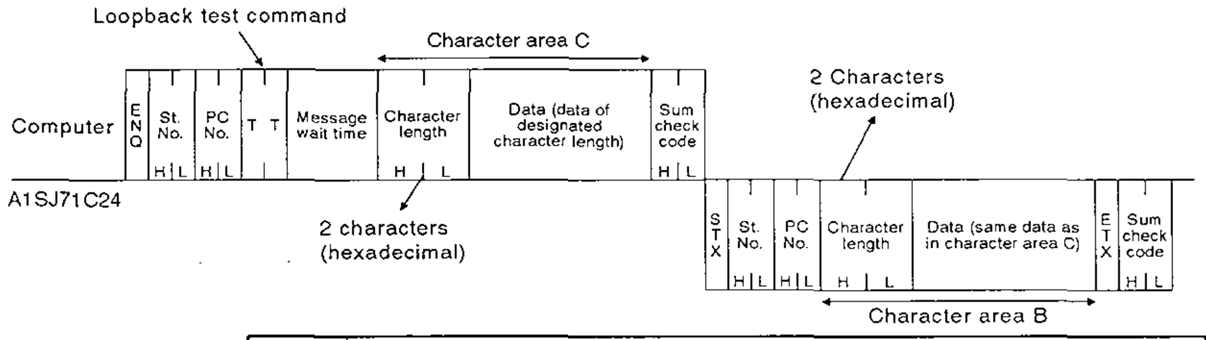
(1) ACPU common command

Item	Command		Processing	Number of Points Processed per Com-munication	State of PC CPU			Access to A1S CPU	Access to PC CPU in Data Link
	Sym-bol	ASCII Code			During STOP	During RUN			
						SW04 ON	SW04 OFF		
Loop-back test	TT	54H, 54H	Echoes back the characters to the computer as they are received	254 characters	○	○	○	○	○

(2) Designating the loopback test

Designation Method

Designation in protocol 1 is shown below.



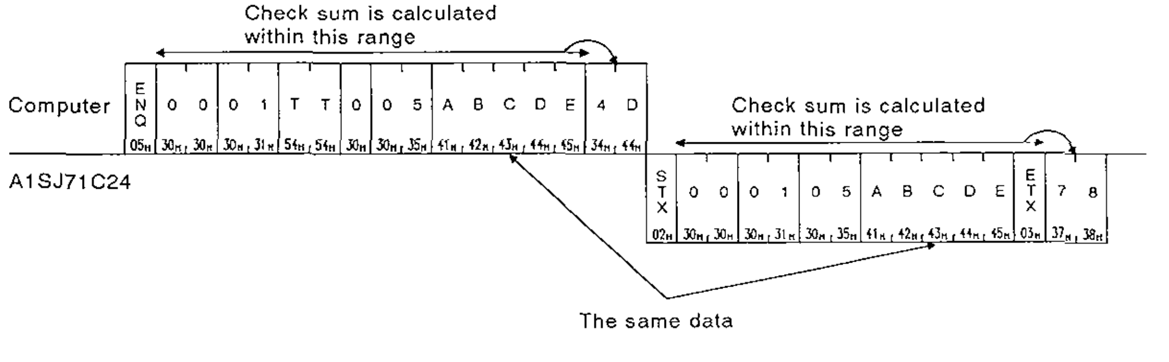
POINT

To set the characer length, the following condition must be met:

- 1 ≤ character length ≤ 254

Designation Example

To execute the loopback test with the "ABCDE" at PC number "01". (Message wait time is 0 msec.)



9. COMMUNICATIONS WITH A COMPUTER IN THE NO-PROTOCOL MODE

Read this chapter when the RS-232C interface with the no-protocol mode by setting the mode setting switch at the A1SJ71C24 in position of "5".

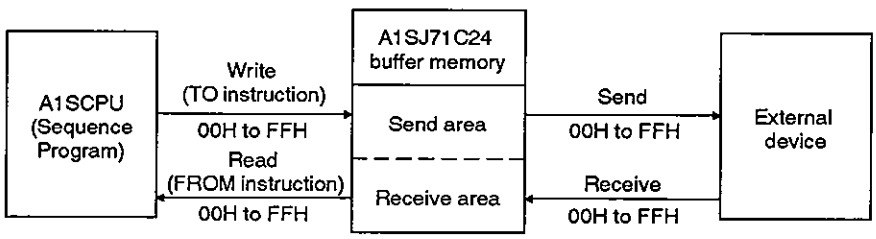
If these interfaces are used with the dedicated protocol and in the bidirectional mode, it is not necessary to read this chapter.

9.1 Basics of the No-Protocol Mode

(1) What no-protocol mode means

In no-protocol communication:

- Data written to the no-protocol A1SJ71C24 send area (in buffer memory) using the TO instruction in a sequence program is output to an external device in the same code.
- Data received from an external device is read from the no-protocol A1SJ71C24 receive area (in buffer memory) using the FROM instruction in a sequence program.



POINT

In the no-protocol mode, data is not converted to ASCII code in the A1SJ71C24. If ASCII code is required, the data must be processed into ASCII code in the A1SCPU.

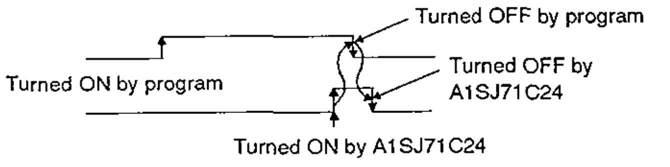
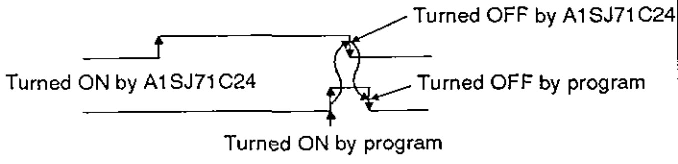
(2) Designating a word/byte unit for no-protocol mode communication

For data communications in the no-protocol mode, a unit of data to be transmitted may be selected between words and bytes. Default setting for data unit selection is "word", but selection is possible by writing "1" or "0" to address 103H in the buffer memory area.
(Section 7.4.3 gives details about the program to make this setting.)

9.2 Handshake I/O Signals

Signals known as I/O handshake signals are required for no-protocol communications.

These signals (a) output data received from the sequence program to an external device, or (b) detect signals from an external device to enable the sequence program to read them.

	Signal	Timing
A1SCPU ↓ External device	$Y_{(n+1)}0$ (Send request) X_n0 (Send completed)	
External device ↓ A1SCPU	X_n1 (Received data read request) $Y_{(n+1)}1$ (Receive data read completed)	

The letter n attached to X and Y given above is decided by both the slot number of this module and the number of I/O modules installed in the previous slots. (e. g., if an A1SJ71C24 is installed in slot 0 of the main base unit, Xn0 becomes X0.)

9.3 Programming Hints

9.3.1 To write data to the special use area in buffer memory

(1) Buffer memory is not backed up by a battery.

All data in buffer memory is set to the default values when power is turned ON or when the PC CPU is reset. Data changed from the default values must be written to the buffer memory whenever the power is turned ON or the CPU is reset.

(2) Only TO instruction can be used to write data to the special use area (100H to 11FH). If data is written to the buffer memory using the command in a computer program, the A1SJ71C24 will not operate correctly. Never try to write data using a computer program.

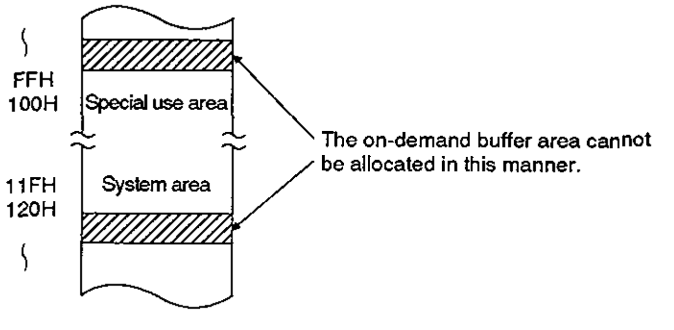
(3) If the following functions are used in combination with the dedicated protocol, make sure to allocate the user area in buffer memory so that the same area will not be used by different functions.

If the same area is allocated to different functions, the data in this area is rewritten and communications will not be correctly executed.

- No-protocol mode transmission or bidirectional mode transmission
- No-protocol mode receive or bidirectional mode receive

The memory areas preceding and following the special use area cannot be allocated as a single area. The areas 0H to FFH and 120H to 7FFH must be recognized as independent areas.

Example)



9.3.2 Precautions during data communications

(1) Conditions when the A1SJ71C24 transmission sequence is initialized

The transmission sequence is initialized in the following cases:

- Power is turned ON or the A1SCPU is reset by the reset switch.
- The A1SJ71C24 CD signal is turned OFF during RS-232C full-duplex communications.

(If the CD signal is turned OFF during send or receive processing, data being processed for transmission or the data stored in the A1SJ71C24 receive data storing OS area is cleared.
In full-duplex communications, keep the CD signal ON.
The ON/OFF status of the CD signal is ignored if "CD terminal check disabled" is set at 10BH of the buffer memory address.)

(2) FROM/TO accesses to an A1SJ71C24

The FROM/TO accesses made by the PC CPU to an A1SJ71C24 must be executed only when they are strictly needed.

If a FROM/TO access is made by the PC CPU to an A1SJ71C24 when the A1SJ71C24 is transmitting data to an external device, the FROM/TO instruction is given priority in processing.

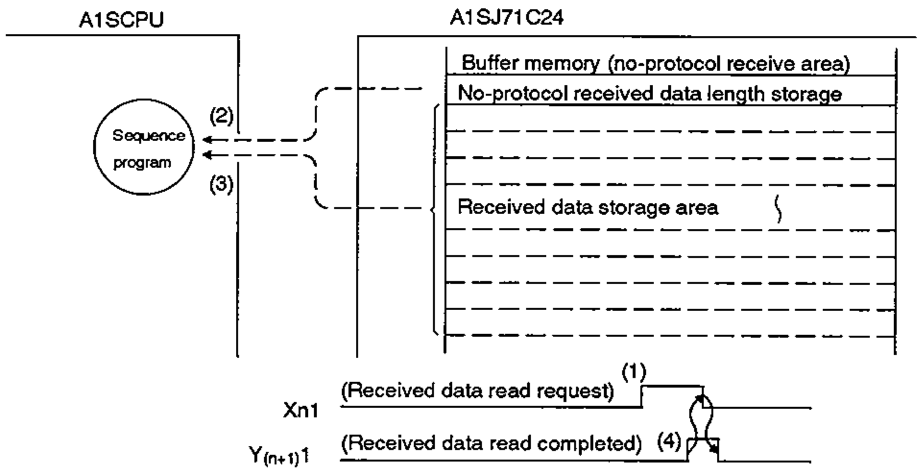
The data transmission time of the A1SJ71C24 accordingly increases since the FROM/TO instruction is processed.

9.4 Basic Program to Read/Write Buffer Memory

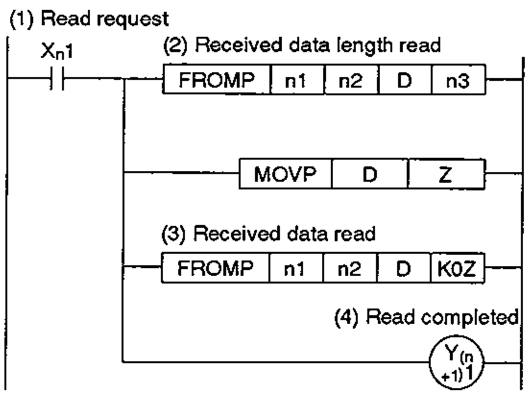
The following describes a basic sequence program to read and write data to and from the A1SJ71C24 buffer memory.

(1) Reading data from the receive area (FROM, FROMP, DFRO, DFROP)

Data is read from the buffer memory no-protocol receive area (default: 80H to FFH).



Format



Reads the received data length from the no-protocol received data length storage area of buffer memory when the read request signal (Xn1) is turned ON.

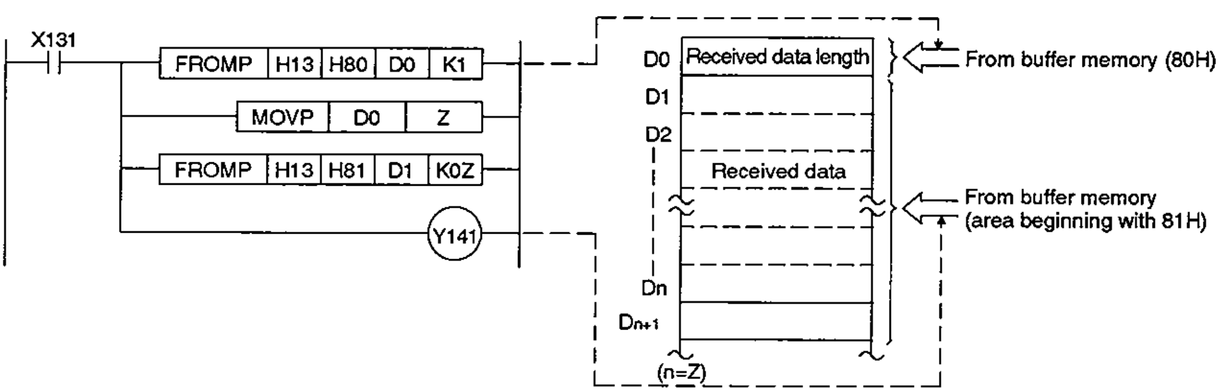
Stores the read data length to the index register (Z).

Reads the received data of the read received data length from the received data storage area of buffer memory.

Turns ON the read completed signal (Y(n+1)1) after the received data has been read

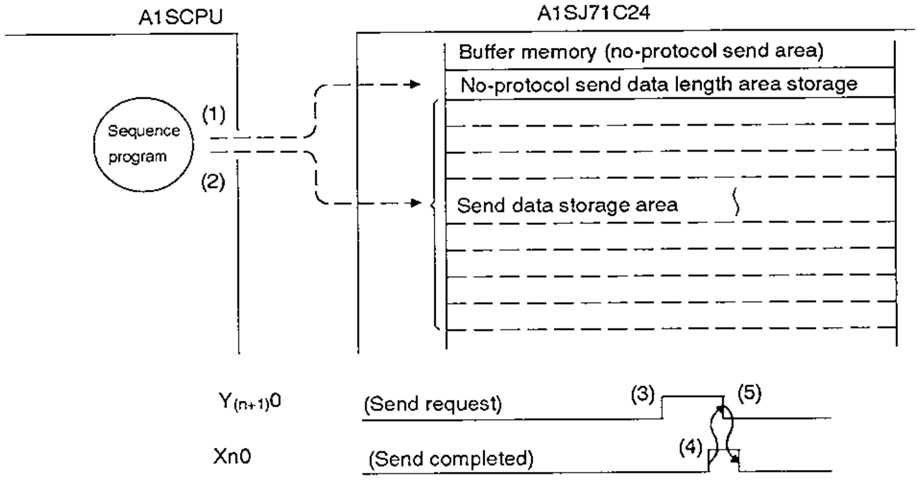
* Data read by program 3) is processed as the received data.

Example: To read the data of (n+1) words from the area, beginning with buffer memory address 80H, to the area beginning with D0 when the A1SJ71C24 I/O numbers are allocated to 130 to 14F.

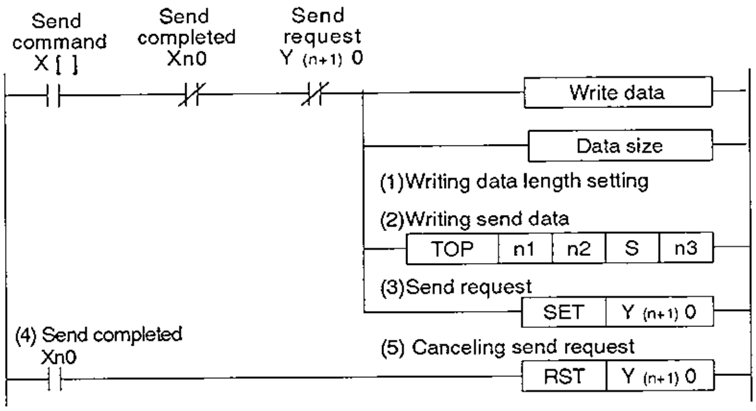


(2) Writing data to the send area (TO, TOP, DTO, DTOP)

Data written to the no-protocol send area (default: 0H to 7FH).



Format



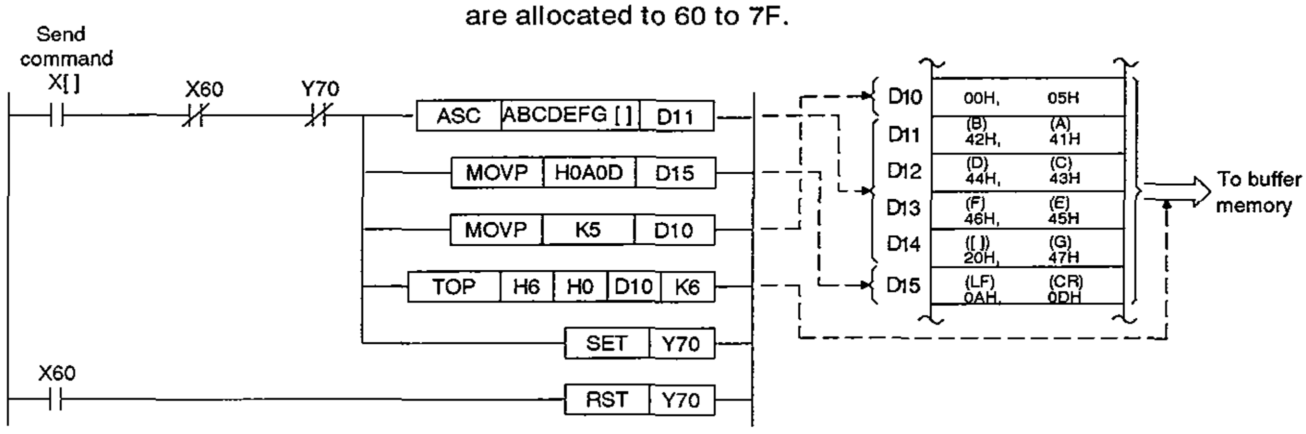
Sets the send data and send data length when the send command signal (X[ ]) is turned ON.

Writes the send data length and send data to the buffer memory.

Turns ON the send request signal (Y(n+1)0) after the data is written.

Turns OFF the send request signal when the data send completed signal (Xn0) is turned ON.

(Example): *To transmit 5-word data after writing "ABCDEFG [ ] CR.LF" to the* buffer memory area from 1H when the A1SJ71C24 I/O numbers are allocated to 60 to 7F.



9.5 Receiving Data in the No-Protocol Mode (External Device → A1SJ71C24)

(1) Data receive area

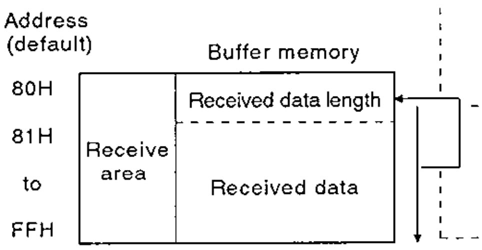
The A1SJ71C24 stores the received data length and received data in the data receive area.

With default setting, buffer memory area 80H to FFH is allocated as the receive area.

This area may be changed as needed. See Section 6.4.5 for the procedure to change the data receive area.

For example, if the data to be received is greater than the A1SJ71C24 receive area (127 words in default setting), data is received in more than one transmission.

It is advisable to set as "data receive area" is larger than "received data length".



The unit (word/byte) of received data length depends on the setting with the word/byte setting area (address 103H).

The actual length of received data is written when the receive completed code is received or the set length of data has been received.

Received data is stored sequentially from the lowest address until the completed code is received or the set length of data has been received.

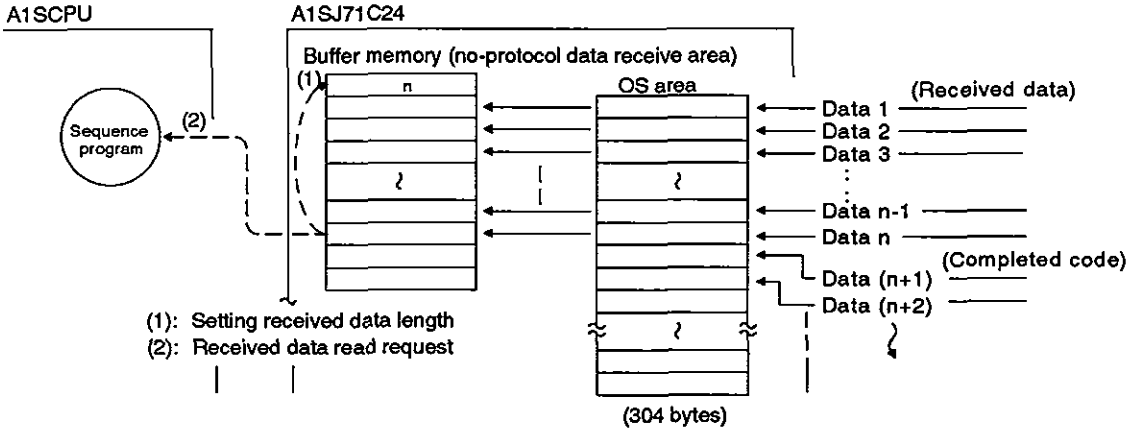
(2) Reading received data

There are two ways of making a request to read the received data:

- By receiving the receive completed code (data receive in variable length), and
- By receiving the set length of data (data receive in fixed length).

(a) By receiving the receive completed code (variable length)

The A1SJ71C24 makes a request to read the received data to the sequence program when it receives the receive completed code, predetermined by the user and set to the A1SJ71C24 buffer memory. The default receive completed code is CR, LF (0D0AH), but this may be changed to any value in the range of 0000H to 00FFH. (For the procedure to change the read completed code, see Section 7.4.1.)

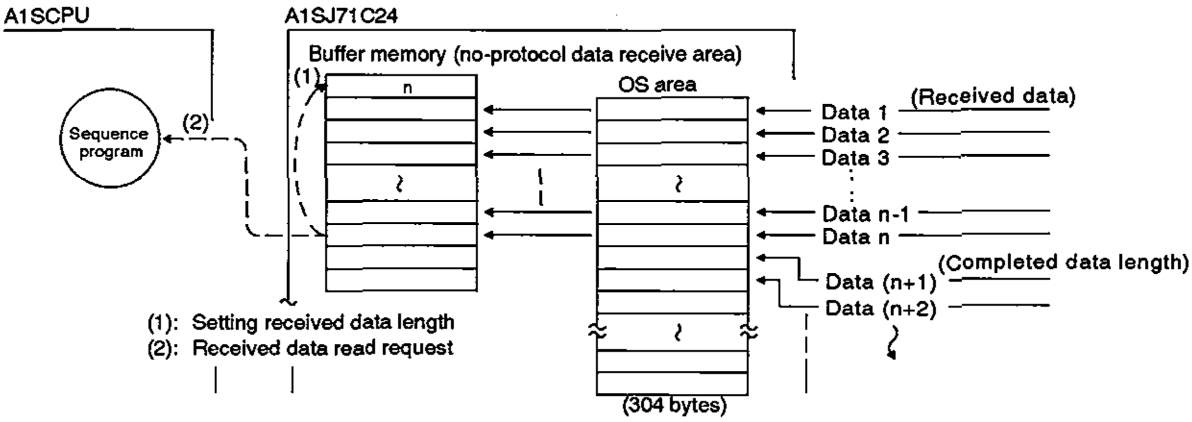


(b) By receiving the set data length (fixed length)

The A1SJ71C24 makes a request to read the received data to the sequence program when it has received the set length of data from an external device.

Using this method, it is possible to receive fixed length data.

Default setting is 127 words, but this value may be changed as required. (For the procedure to change the data length setting, see Section 7.4.2.)



POINTS

(1) When both the receive completed code and the receive completed data length are set to the special application area in buffer memory, both of them are effective.

In this case, the one which is met first triggers the read request signal (Xn1) to the sequence program. See Section 7.4.1 and 7.4.2.

(2) The data received after the reception of the receive completed code or the set length of data has been received is stored in the OS area (304 bytes) of the A1SJ71C24. The data stored in the OS area is transferred to the data receive area after the data previously stored in this area has been read by the sequence program.

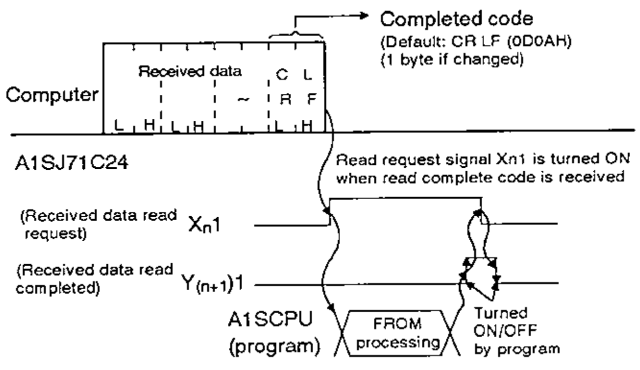
When the size of the vacant area in the OS area, where received data is stored, becomes smaller than 10 bytes, the following control operations are executed according to preset transmission control specifications.

When the DTR control has been set: the A1SJ71C24 turns OFF the DTR signal and makes a request to terminate the send from the communicating equipment (see Appendix 5).

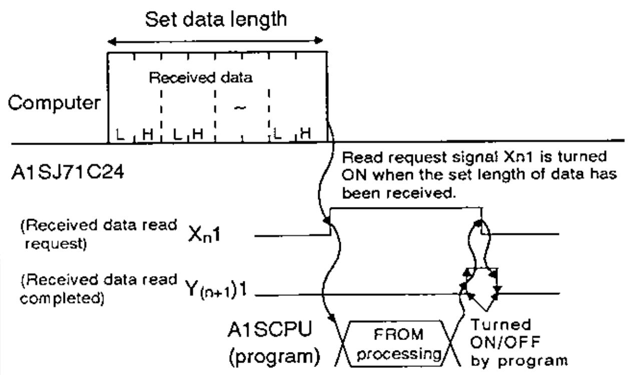
When the DC1-DC3 code transmission control has been set: the A1SJ71C24 sends a DC3 code and makes a request to terminate the send from the communicating equipment (see Appendix 5.1).

(3) Data receive procedure

Reading data by the read completed code



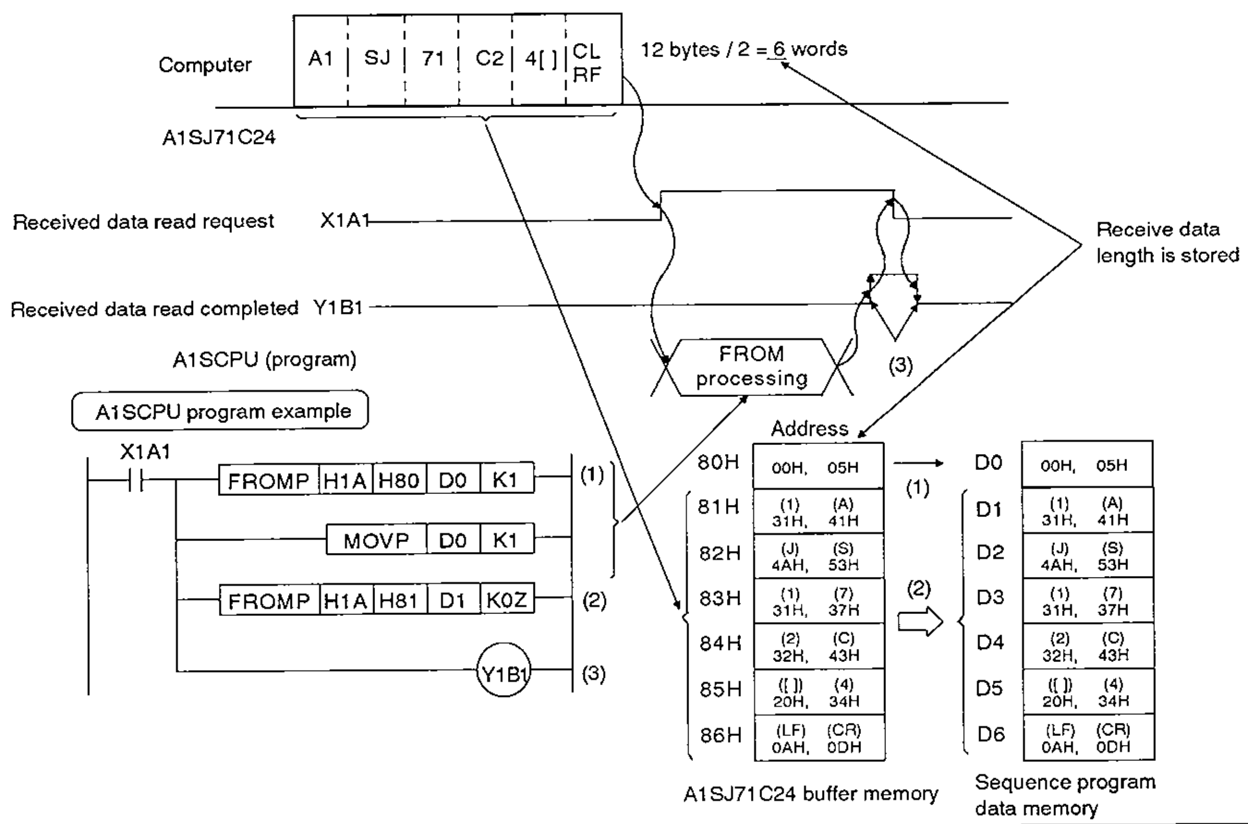
Reading data by the set data length



(4) Data receive program examples

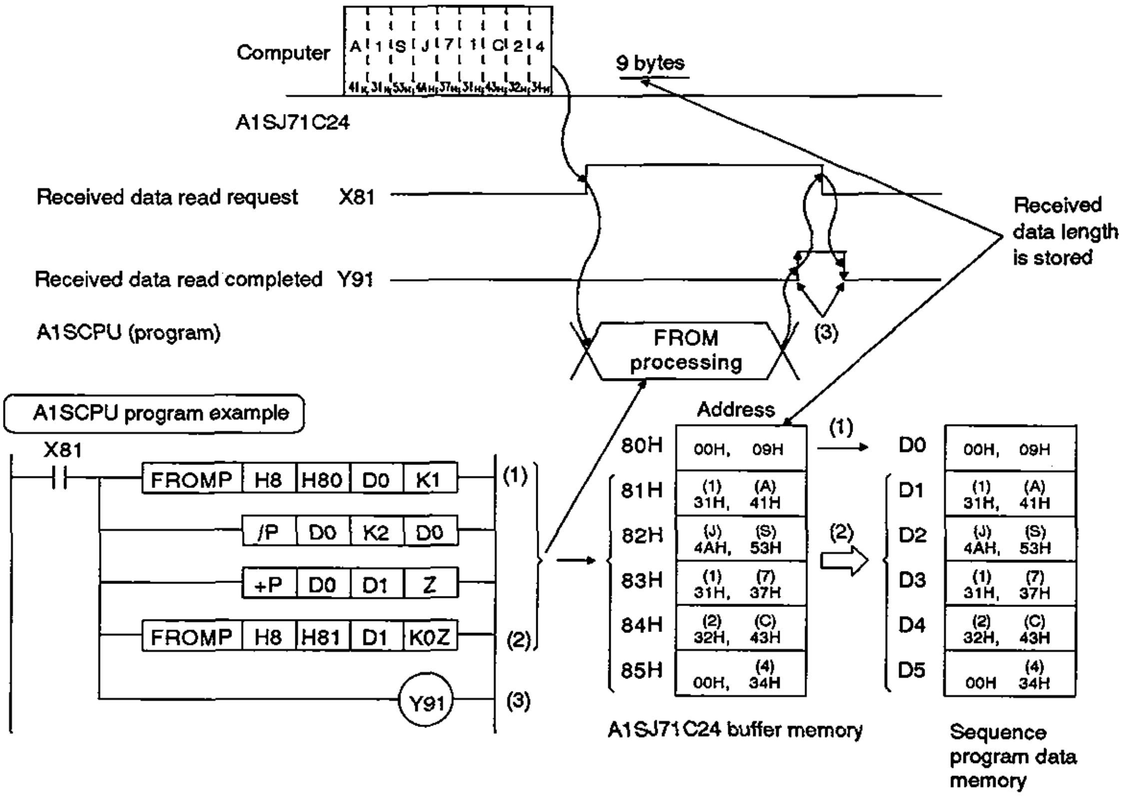
Example 1 : By receiving completed code, in word units (buffer memory allocation: default)

To store "A1SJ71C24[ ]" CR, LF, received from an external device, to D0 to D6 of A1SCPU.
(A1SJ71C24 I/O addresses: 1A0 to 1BF)



Example 2: By receiving the set length of data, in byte units (receive area allocation default)

To receive "A1SJ71C24" from an external device and to store it to D0 to D5 of A1SCPU with the following setting. (A1SJ71C24 I/O address: 80 to 9F)



POINTS

- Even if transmission data units are set to byte units, the FROM instruction in a sequence program operates in word units. Therefore, the length of receive data must be converted to the number of buffer memory points (word units).

  In the above example, 9 bytes of data must be converted into 5 words (9 ÷ 2 = 4.5...5).

- When an odd number of bytes of data is received, the higher 8 bits of the last address read by the FROM instruction are "00H".

REMARKS

If the receive data length exceeds the no-protocol mode receive buffer memory size, the data is processed as described below.

(1) When the receive completed code is used:

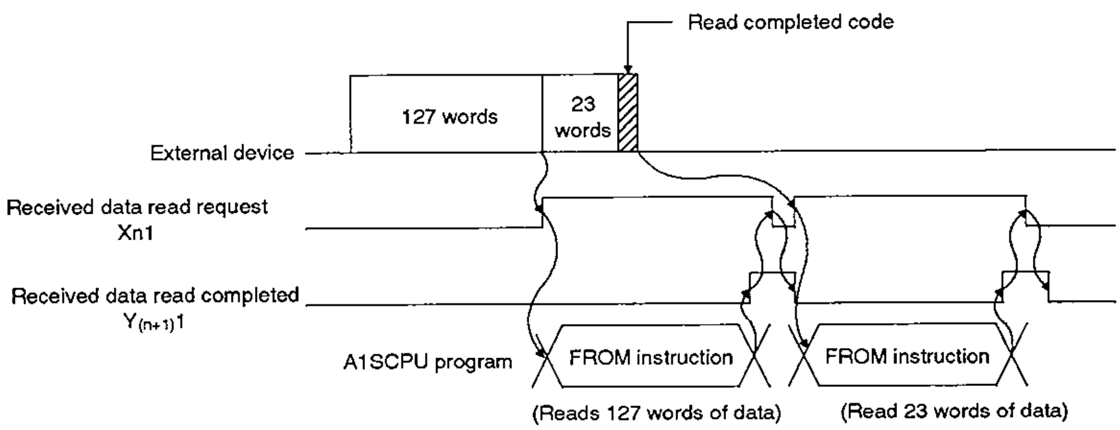
If the A1SJ71C24 receives data that exceeds the receive area size, it turns ON the received data read request signal Xn1 when data equivalent to the receive area size has been received.

Reading the remaining data is enabled at the time the sequence program turns the receive data read completed signal Y(n+1)1 ON.

These steps are repeated until the receive completed code is received.

Set the receive area size so that "receive-completion data length" is less than "no-protocol mode receive buffer memory size".

Example: To receive 150 words of data while receive area is set at 80H to FFH (default).

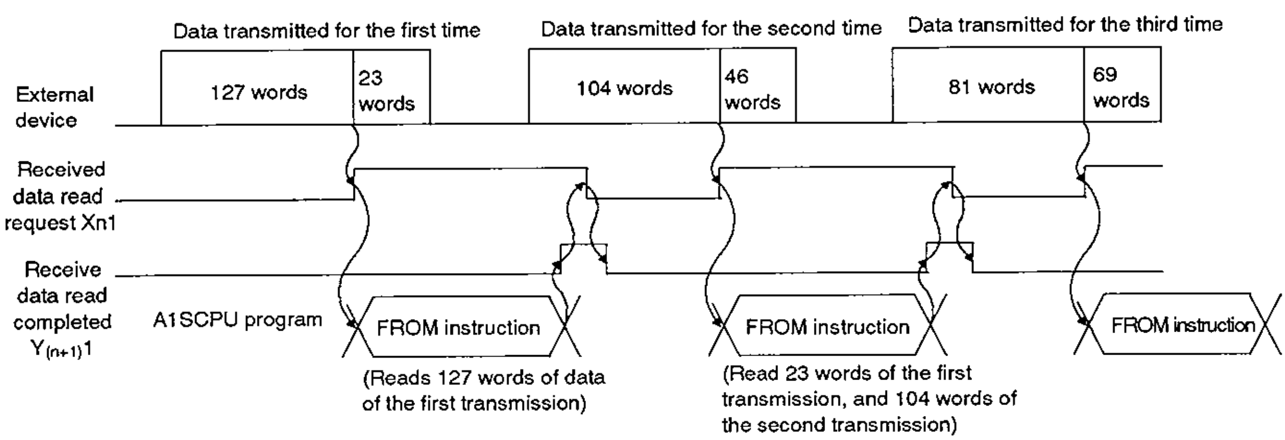


(2) When receive completion data length is used:

If the receive completion data length is set greater than the receive area size, the no-protocol receive buffer memory size (default: 127 words) which is set at buffer memory address 107H is taken as the receive completion data length.

Set the receive area size so that "receive completion data length" is less than "no-protocol mode receive buffer memory size".

Example: To receive 150 words of data while receive area is set at 80H to FFH (default setting).



(5) Clearing the receive buffer memory

If and error occurs due to failure of an external device, for example, while receiving data from an external device in the no-protocol mode, the data received up to the error may be incorrect or interrupted. To received up to the error may be incorrect or interrupted. To recover after an error has occurred it is possible to cleaa all received data and initialized the A1SJ71C24 buffer memory.

(a) Error detection

The following methods are used to detect errors while data is being received.

1) Reading the error LED display area

To detect errors the A1SCPU can read the LED ON/OFF statuses, stored at buffer memory address 101H as transmission error data.

2) PC input signals

Signals such as READY signals from external devices are connected to the A1SCPU as input signals. The A1SCPU can detect errors from the ON/OFF status of these signals.

(b) Clearing receuved data

1) Range of data cleared

All data already received by the A1SJ71C24 is cleared and the no-prptocol mode receive buffer memory area is initialized (See Appendix 5 for details).

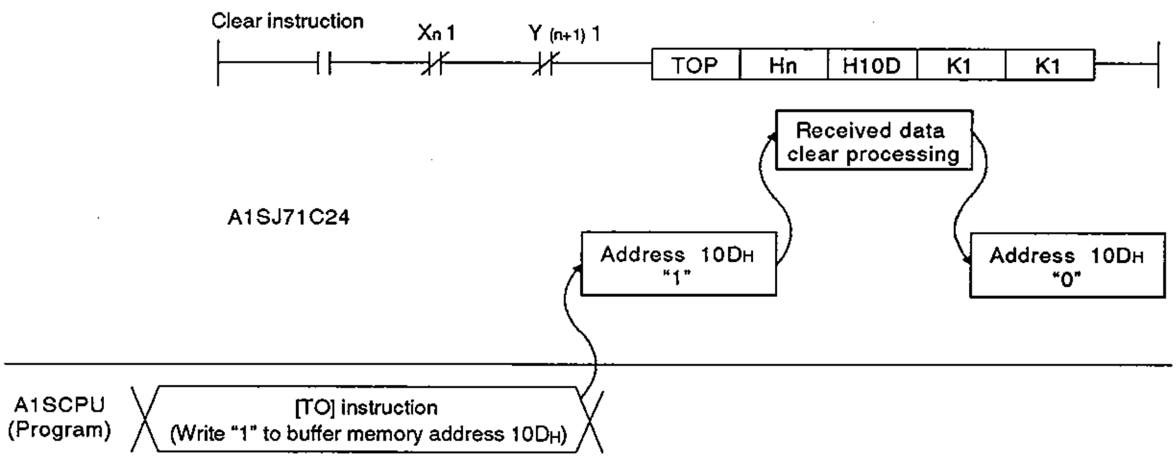
2) How to clear received data

Received data is cleared by writing "1" to buffer memory address 10DH using the [TO] instruction.

After clearing received data, the A1SJ71C24 clears the "1" that was written to buffer memory address 10DH.

The received data may be cleared while the receive data read request signal (Xn1) and received data read completed signal (Y(n+1)1) are OFF.

Use Xn1 and Y(n+1)1 as an interlock for TO instruction.



9.6 Sending Data in the No-Protocol Mode (A1SJ71C24 → External Device)

In this section, "sending" means outputting data which is in the no-protocol mode A1SJ71C24 send area to an external device receive area. This is in response to turning the A1SCPU send request signal (Y(n+1)0) ON.

(1) Send area and writing send data

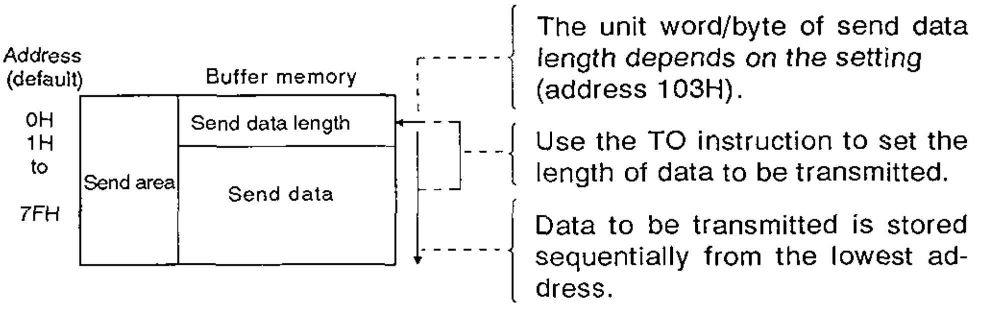
The send data length and send data are written to the send area.

(a) The length of send data to be written (or having been written) to the send data storage area is written to the no-protocol send data length storage area in either words or bytes.

(b) The data to be transmitted is written to the send data storage area.

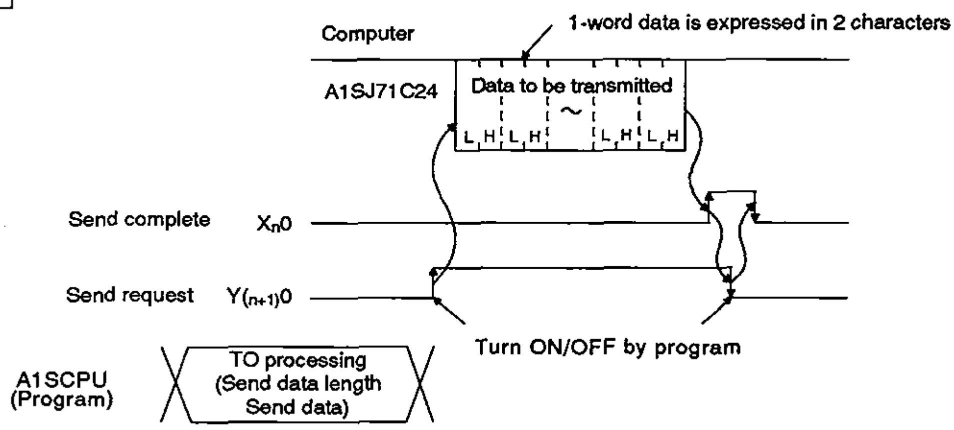
When the send request signal (Y(n+1)0) is turned ON after (a) and (b) have been executed, the A1SJ71C24 transmits the set length of set data from the send data storage area in the order of address number.

By default, buffer memory area 0H to 7FH is allocated to the A1SJ71C24 send area.
It is however possible to change the send area allocation. (See Section 7.4.4.)



(2) Data sending procedure

Procedure



POINTS

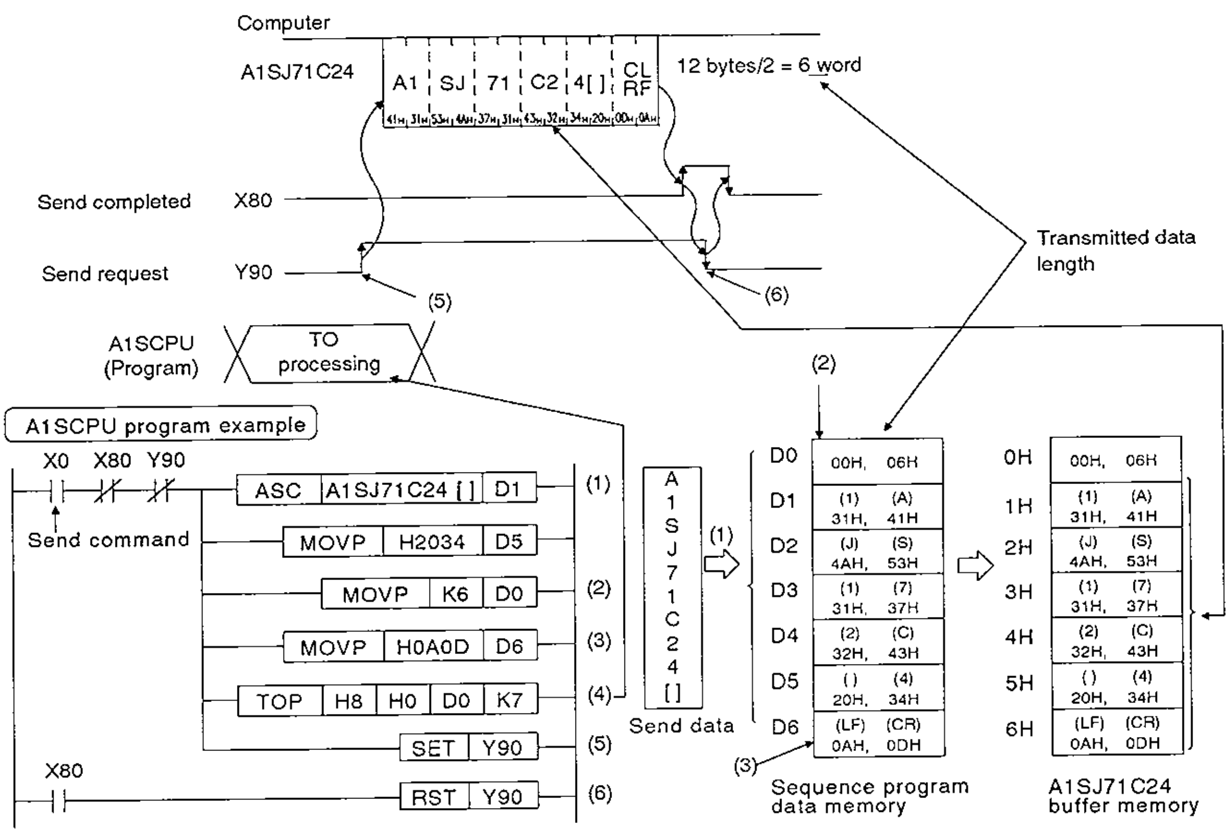
(1) An error occurs if the send data length is greater than the send area, or equal to "0". In this case, "1" is written as transmission error information to the most significant bit (bit 15) of address 101H (error LED display area) in the special application memory area. (See Section 7.3.1.)

(2) The send data length written to the head address of the send area is not transmitted.

(3) Data transmission program examples

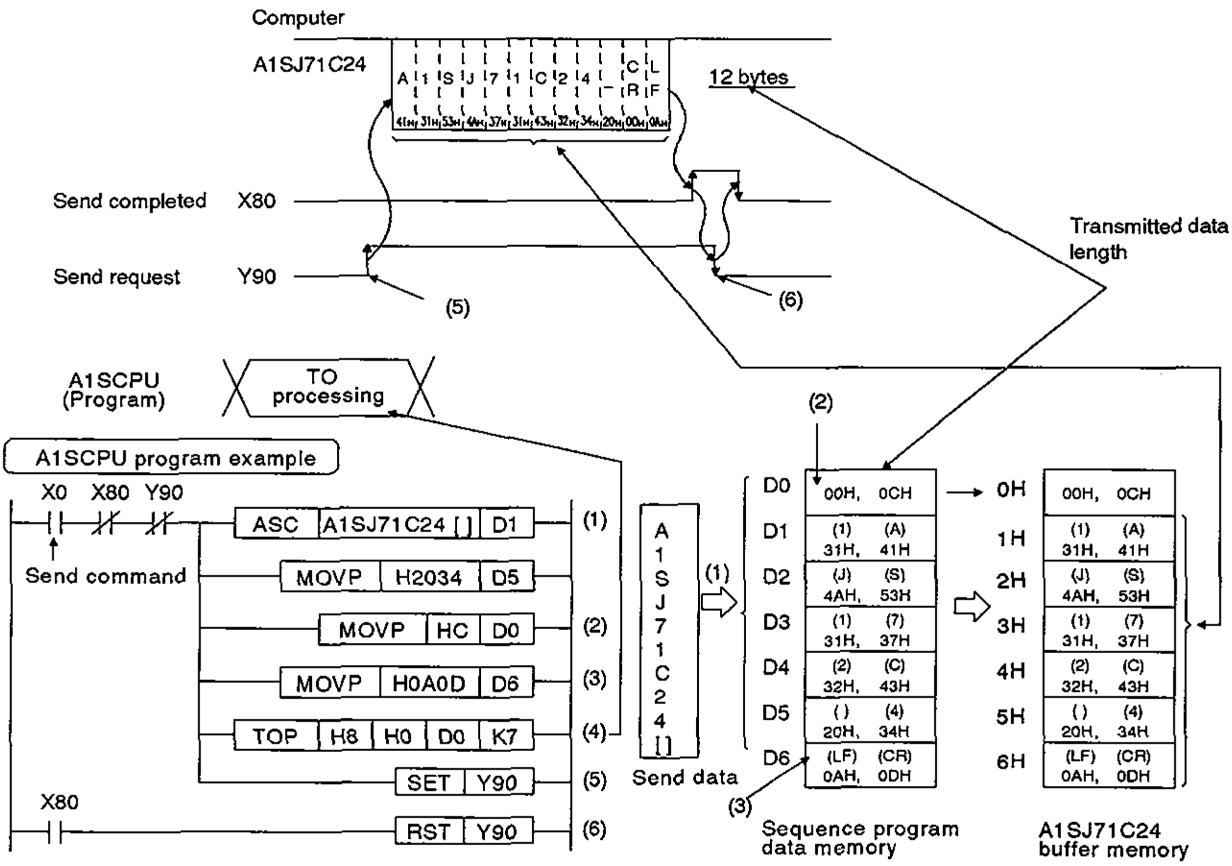
Example 1: Transmitting data in word units (buffer memory allocation: default)

To write "A1SJ71C24[ ]"CR, LF by sequence program and transmit it to an external device (A1SJ71C24 I/O addresses: 80 to 9F)



Example 2: Transmitting data in word units (buffer memory allocation: default)

To write "A1SJ71C24[ ]"CR, LF by sequence program and transmit it to an external device (A1SJ71C24 I/O addresses: 80 to 9F)



POINT

Even if transmission data units are set byte units, the TO instruction in a sequence program operates in word units. Therefore, the length of send data differs from the data length set with the TO instruction.

10. COMMUNICATIONS IN THE BIDIRECTIONAL MODE

Always read this section when the RS-232C interface is used with the bidirection mode individually by setting the mode setting switch at the A1SJ71C24 in position of "5" .

It is not necessary to read this section when the interface is used with the dedicated protocol and in the no-protocol modes.

POINT

Buffer memory used in the bidirectional mode

In sections other than this, buffer memory used in the bidirectional mode is described as the buffer memory used for the no-protocol mode. Because the application purposes are the same, simply think of the "no-protocol mode" as the "bidirectional mode".

Examples:

- No-protocol mode send area
  → Bidirectional mode send area
- No-protocol send buffer memory head address setting area
  → Bidirectional send buffer memory head address setting area

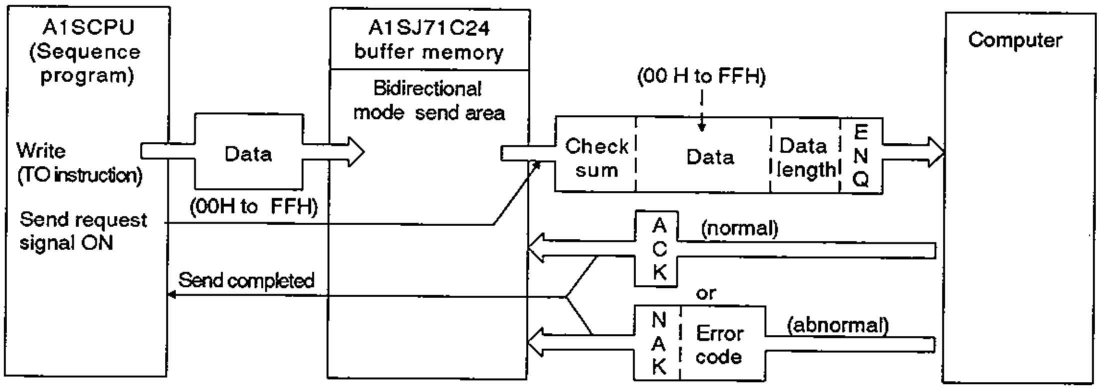
10.1 Bidirectional Mode Basics

(1) What bidirectional mode means

In bidirectional communications:

The bidirectional receive/send area in an A1SJ71C24 buffer memory is used for data commumications with a computer.

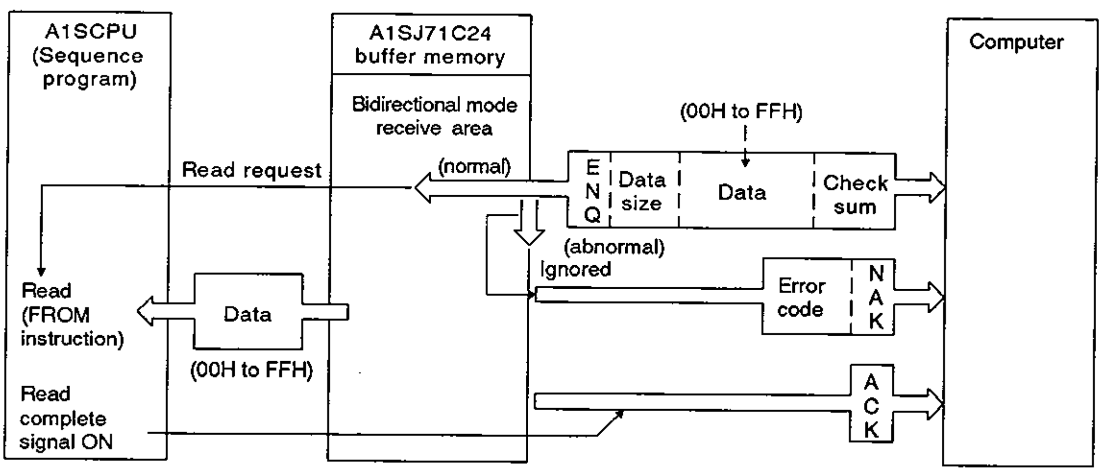
The data written to an A1SJ71C24 buffer memory by the TO instruction in a sequence program is transmitted to a computer in the same code with the control code (ENQ=05H) prefixed to the data to be transmitted.



An A1SJ71C24 receives a response from a computer.

The data received from a computer is stored in an A1SJ71C24 received area and read by the FROM instruction in the sequence program (the data received is transferred in the code as received).

The response data is transmitted to a computer in response to the read completed signal.



POINT

In the bidirectional mode, data is not converted to ASCII code in the A1SJ71C24. If ASCII code is required, the data must be processed into ASCII code in the A1SCPU.

(2) Designating word/byte units for bidirectional mode communications

For data communications in the bidirectional mode, units of data to be transmitted may be selected between words and bytes. Default setting for data unit selection is "word", but selection is possible by writing "1" or "0" to address 103H in the buffer memory area.

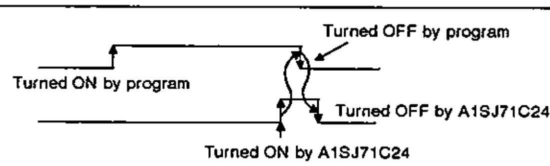
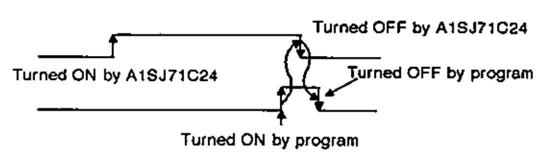
(Section 7.4.3 gives details of the program to make this setting.)

10.2 Handshake Signals and Buffer Memory

(1) Handshake signals in the bidirectional mode

Signals known as I/O handshake signals are required for communications in the bidirectional mode.

These signals output data received from the sequence program to a computer or detect signals from an external device to enable the sequence program to read them.

	Signal		Timing
A1SCPU ↓ Computer	Y (n+1) 0	(Send request)	
	X n 0	(Send completed)	
Computer ↓ A1SCPU	X n 1	(Received data read request)	
	Y (n+1) 1	(Receive data read complete)	

The number "n" appended to X and Y is determined according to the position where the A1SJ71C24 is loaded and the number of I/O modules loaded prior to this module. If this module (A1SJ71C24) is loaded at slot 0 in a base module, Xn0 is expressed as "X0".

(2) Buffer memory used in the bidirectional mode

(a) *Special applications area (100H to 1FFH)*

Address	Name	Description
103H	Word/byte designation area for bidirectional mode	• The unit (word/byte) of data length of a message transmittted between a computer and a PC CPU is designated with a TO instruction in a sequence program. This sets the unit of data to be stored in the send data length storage area (default address 0H) and the received data length storage area (default address 80H). 0: Word (default) 1: Byte
104H	Bidirectional mode send buffer memory area head address designation area	• The head address of the area used for bidirectional mode send buffer memory area (send data length storage area and send data strage area) is designated with a TO instruction in a sequence program. • The area of the designated address is set as the send data length storage area. (0 to FEH or 120H to 7FEH : Bidirectional send buffer memory head address. (default : 0H)
105H	Bidirectional mode send buffer memory length designation area	• The length of the area used for bidirectional mode send is designated with a TO instruction in a sequence program. (default: 80H). When 0H to FFH area is used, 2H to 100H: Bidirectional send buffer memory When 120H to DFFH area is used, 2H to CE0H: Bidirectional send buffer memory length
106H	Bidirectional mode receive buffer memory area head address designation area	• The head address of the area used for bidirectional mode receive buffer area (receive data length storage area and receive data storage area) is designated with a TO instruction in a sequence program. • The area of the designated address is set as the receive data length storage area. 0H to FEH or 120H to 7FEH:Bidirectional mode receive buffer memory head address. (default: 80H)
107H	Bidirectional mode receive buffer memory length designation area	• The length of the area used for bidirectional mode data receive is designated with a TO instruction in a sequence program (default: 80H). When 0H to FFH area is used, 2H to 100H: Bidirectional receive buffer memory length When 120H to DFFH area is used, 2H to CE0H: Bidirectional receive buffer memory length

(continued on page 10-6)

(continued)

Address	Name	Description
112H	Bidirectional mode designation area	• Whether the interface communications mode is no-protocol or bidirectional is designated with a TO instruction in a sequence program. 0: No-protocol mode (default) 1: Bidirectional mode
113H	Time-out check time designation area	• The time-out check time (until the reception of a response after transmission of data to the computer) is designated with a TO instruction in a sequence program. 0H : Time-out is not checked (default) 1H to FFFFH : Time-out check time (100 msec units) The most significant bit in the area is not regarded as the sign bit. The set value is regarded to designate value in the range of 1 through 65535.
114H	Data valid/invalid designation area at simultaneous transmission	• How the receive and send data at an A1SJ71C24 is processed if data transmission at a computer and an A1SJ71C24 occurs simultaneously is designated with a TO instruction on a sequence program. (Section 10.6 covers silmultaneous transmission) b15 to b8 b7 to b0 114H (default: 0000H) b7 to b0 → Receive data (00H: valid, 01H: Invalid) b15 to b8 → Send data (00H: valid, 01H: Invalid)
115H	Bidirectional mode check sum enable/disable designation area	• Whether or not check sum is appended for bidirectional mode communications is designated with a TO instruction in a sequence program. (This designation is not related to the setting of DIP switch SW12.) 0: Check sum enabled (default) 1: Check sum disabled
116H	Error storage area for data send	• If an error occurs during data communications, the error code is transmitted by an A1SJ71C24. (The area designated in 117H retains the error code of the last data receive error.) 0H : Normal termination (no error) 0001H to 0082H : Abnormal termination (error) Section 11.2 gives error code details.
117H	Error storage area for data received	

POINT

The area described above is the special applications area for bidirectional mode communications.

For other special applications areas used for data communications, see Section 3.5, section 5, and section 7.

(b) User areas (0H to FFH and 120H to DFFH)

Address	Name	Description
0H to FFH and 120H to DFFH	Send data length storage area	• The length (words or bytes) of data written to the send data storage area, to be transmitted from the A1SJ71C24 to the computer, is designated with a TO instruction in a sequence program • The set value is used as it is to designate data length in a message to be sent to the computer. • The unit of data length is determined by the value set at address 103H. • Set the send data length within the send data storage area length, described below.
	Send data length storage area	• The data to be transmitted to the computer is designated with a TO instruction in a sequence program. • The buffer memory length and length of the send data and send data length storage areas are determined by the values set at 104H to 105H. (Default: Send data length storage area address : 0H Send data storage area address : 1H to 7FH)
	Received data length storage area	• The data length in the message received from the computer is written *by an A1SJ71C24 as it is as the received data length.* Data length expresses the number of words/bytes at the data section in the message. • The unit of data length is determined by the value set at address 103H. • Transmit the data from the computer within the receive data storage area length described below.
	Received data length storage area	• The data in the data section in the message received from a computer is transmitted by the A1SJ71C24 as it is received. • The buffer memory length and length of the received data and received data length storage areas are determined by the values set at 106H to 107H. (Default: Received data length stora area address : 80H Received data storage area address : 81H to FFH)

10.3 Programming Hints

10.3.1 System configuration and communications mode for bidirectional mode communications

System configuration and the A1SJ71C24 mode setting

The mode setting switch in the A1SJ71C24 should be set in position of "5" .

10.3.2 To write data to a special applications area in buffer memory

(1) Buffer memory is not battery backed up by a battery

All data in buffer memory is set to the default values when power is turned ON or when the A1SCPU is reset.

The data changed from the default values must be written whenever the power is turned ON or the A1SCPU is reset.

(2) Only TO instruction can be used to write data to the special applications area (100H to 11FH).

(3) If data is written using the command in a computer program, the A1SJ71C24 will not to operate correctly. Never try to write data using a computer program.

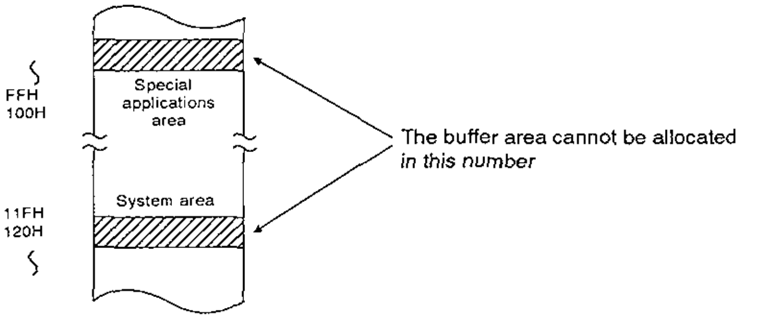
If the following functions are used in combination with the dedicated protocol, allocate the user area in buffer memory so that the same area will not be used by different functions.

If the same area is allocated to different functions, the data in this area is rewritten and communications will not be correctly executed.

- Bidirectional mode send
- Bidirectional mode receive

The memory areas preceding and following the special applications area cannot be allocated as a single area. The areas of 0H to FFH and 120H to DFFH must be recognized as independent areas.

Example:



10.3.3 Precautions during data communications

(1) The conditions under which the A1SJ71C24 transmission sequence is initialized are as follows:

- The power supply is turned ON or the A1SCPU is reset with the reset switch.
- Data communications has completed normally.
- The response message (ACK or NAK) is transmitted.
- During full-duplex communications through the RS-232C interface, the CD signal is turned OFF.

(The ON/OFF status of the CD signal is ignored if the CD terminal check function is disabled.)

(2) Send request signal made by the computer

To transmit data from an A1SJ71C24 send area to a computer receive area, follow the steps described in Section 10.9.

Once the send request signal (Y(n+1)0) is turned ON, do not turn it OFF until the send completed signal (Xn0) is turned ON.

When the send request signal is turned OFF by turning ON the send completed signal, read the error code storage area (116H) for data transmission to check the send result.

(3) Data send from the computer send area or A1SJ71C24 send area

To transmit data from a computer or A1SJ71C24 in the bidirectional mode, start data communications in sequence only after the receive/send of the response for the previous data send/receive has been completed.

(4) Data length

The data length in a message must be smaller than the send or receive data storage area that is set at the special applications area.

(a) Data transmitted from an A1SJ71C24 send area to a computer-receive area

Data length must be smaller than the send data storage area length [(set value at buffer memory address 105H) - 1 (words)].

(b) Data transmitted from a computer send area to A1SJ71C24 receive area

Data length must be smaller than the received data storage area length [(set value at buffer memory address 107H) - 1 (words)].

(5) NAK code

(a) Transmitting NAK from an A1SJ71C24 to a computer

The NAK response is given from an A1SJ71C24 to a computer if an error is detected.

Therefore, the NAK response might be given while the computer is transmitting data if communications is made in the full-duplex mode.

(An A1SJ71C24 ignores the designated length of received data if it detects an error while receiving data. If the data length is incorrect, the data received is ignored until the ENQ code is received.)

(b) Transmitting NAK from a computer to an A1SJ71C24

To transmit the NAK from a computer to an A1SJ71C24, transmit a 2-byte error code following the NAK code.

If the NAK code is received as the response, execute error processing according to the error code received directly after the NAK code.

The error codes related to the bidirectional mode communications are described in Section 11.2.

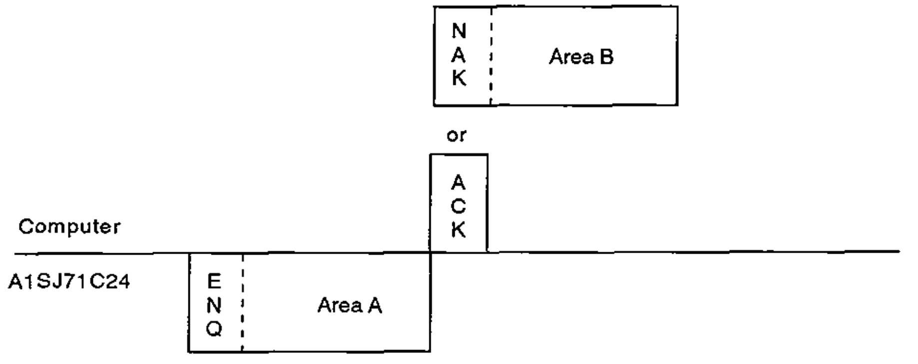
(6) Time-out check by a computer

If a time-out check is made for data transmitted from a computer send area to an A1SJ71C24 receive area in the bidirectional mode, the time-out check time to be set must be longer than the value shown below.

(Maximum scan time of the A1SCPU x 2) + 100 msec

10.4 Bidirectional Control Procedure Basics

(1) Transmitting data from an A1SJ71C24 to a computer

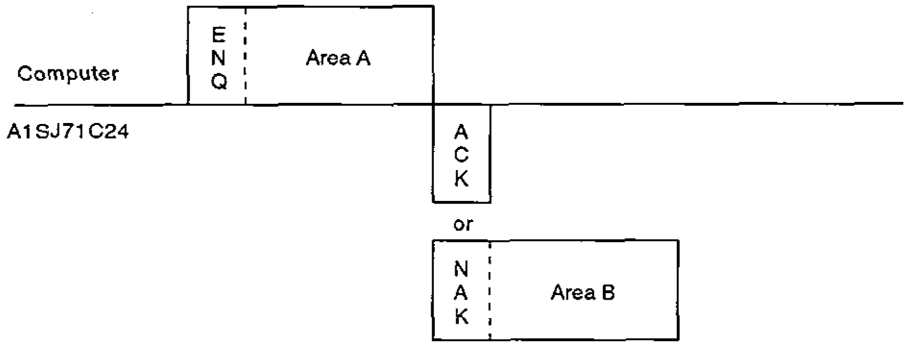


(a) Area A: Data send from an A1SJ71C24 to a computer

(b) Area B: Data send from a computer to an A1SJ71C24

(c) Write a program so that data is transmitted from left to right.
(Example: For area A, data is transmitted from ENQ to right)

(2) Transmitting data from a computer to an A1SJ71C24



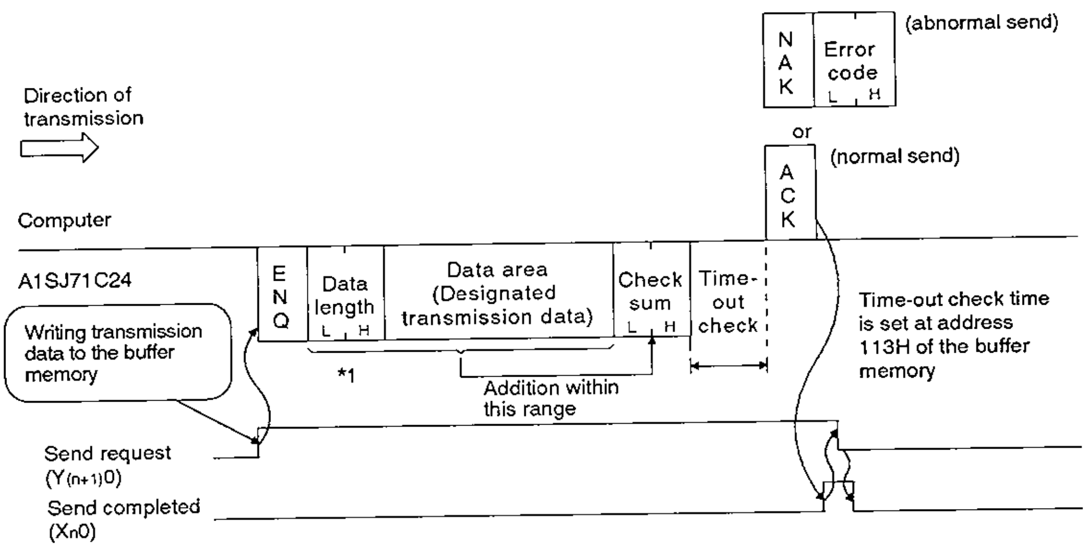
(a) Area A: Data send from a computer to an A1SJ71C24

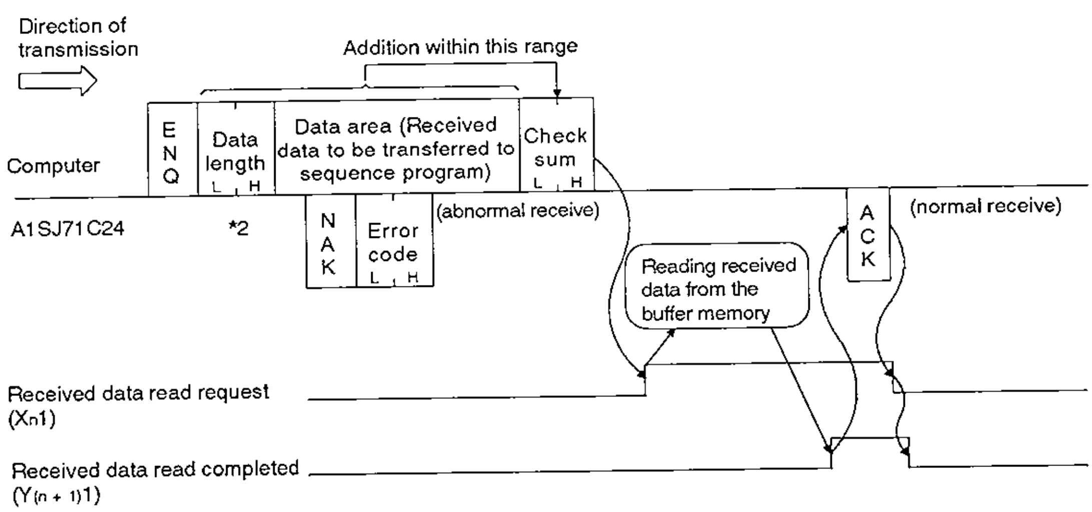
(b) Area B: Data send from an A1SJ71C24 to a computer

(c) Write a program so that the data is transmitted from left to right.
(Example: For area A, data is transmitted from ENQ to right)

10.5 Bidirectional Communications Basics

10.5.1 Control protocols

<table>
<tr><th>Contents</th><th>Protocol</th></tr>
<tr><td>Transmission from a A1SCPU to a computer</td><td>


</td></tr>
<tr><td>A A1SCPU receives data from a computer</td><td>


</td></tr>
<tr><td>Remark</td><td>(1) Check sum exists only when "0" is set to address 115H of buffer memory.
(2) Check sum is calculated within the area indicated by *1.
(3) The A1SJ71C24 returns an NAK immediately if it detects an error as in *2 while communications is made in the full-duplex mode. In half-duplex mode communication, it returns an NAK only after the data has been received.
The A1SJ71C24 ignores receive data if it detects an error (Section 10.3.3 (5)). Therefore, it does not give a received data read request to the A1SCPU.</td></tr>
</table>

10.5.2 Message format

(1) Control code

Signal Name	Code (hexadecimal)	Meaning	Application
ENQ	05H	Enquiry	The code used to begin data send.
ACK	06H	Acknowledge	The code returned to the mating station when data has been received correctly.
NAK	15H	Nagative Acknowledge	The code returned to the sending stations when data has not been receiving correctly. (immediately followed by an error code)

(a) Data send from an A1SJ71C24 to a computer

The A1SJ71C24 appends the control code to be transmitted.

(b) Data send from a computer to an A1SJ71C24

The A1SJ71C24 checks the control code received. It is not possible to read the control code from a sequence program.

(2) Data length

Data length expresses the number of bytes or words of data in the data area in 2-byte binary data. Data length units are determined according to the setting at address 103H of the buffer memory.

(a) Data send from an A1SJ71C24 to a computer

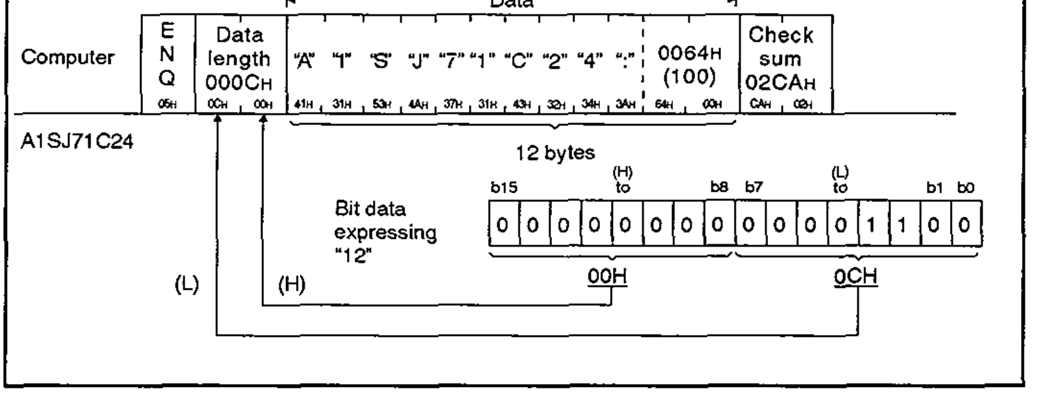
The data length to be transmitted is the value written to the send data length storage area of the A1SJ71C24 buffer memory by the TO instruction in a sequence program.

The A1SJ71C24 transmits the written value as it is from the lower byte (L).

(b) Data send from a computer to an A1SJ71C24

The A1SJ71C24 checks the received data length. When it is correct, the A1SJ71C24 writes the first 1 byte to the lower byte position (L) of the received data length storage area of the A1SJ71C24 buffer memory.

Example: Data length when transmitting "A1SJ71C24:" and value "100" (units: bytes)



(3) Data area

The data of 00H to FFH code can be processed in a string of 1-byte data as the send data.

(a) Data send from an A1SJ71C24 to a computer

The data area to be transmitted is the value written to the send data storage area of the A1SJ71C24 buffer memory by the TO instruction in a sequence program.

The A1SJ71C24 transmits the data according to the designated length and byte/word units sequentially from the lower address in unchanged codes.

(b) Data send from a computer to an A1SJ71C24

The data area received is written to the received data storage area sequentially from the lower address in unchanged codes as they are received.

The data length to be written is determined by the data length in the received message and the designated word/byte units.

(4) Check sum

The check sum is the lower 2 bytes (16 bits) of the result obtained by adding the data length and the data area in the message as binary data.

If the setting at address 115H is "1", the check sum is not required.

(a) *Data send from an A1SJ71C24 to a computer*

The A1SJ71C24 calculates and adds the check sum.

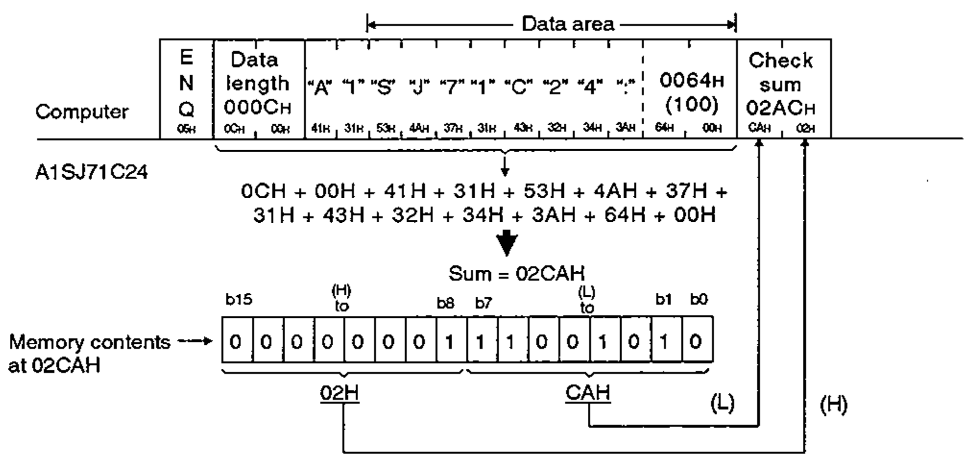
If the check sum is not processed, the check sum is not transmitted.

(b) Data send from a computer to an A1SJ71C24

The A1SJ71C24 checks and processes the check sum received. It is not possible to read the check sum from a sequence program.

When the setting is "check sum is disabled", the received data following the data of the designated length is ignored up to the next control code.

Example: Check sum when transmitting "A1SJ71C24:" and value "100" (units: bytes) is processed as follows.



(5) Error code

An error code indicates the error content when an NAK response is received. The code is transmitted and received in the range of 0001H to 00FFH. Section 11.2 gives error code details.

(a) Data send from an A1SJ71C24 to a computer

The A1SJ71C24 appends the error code.

When transmitting an error code, the A1SJ71C24 writes the same error code to its error code storage area in the received data buffer memory area.

(b) Data send from a computer to an A1SJ71C24

The A1SJ71C24 writes the received error code to the error code storage area in its send data buffer memory area.

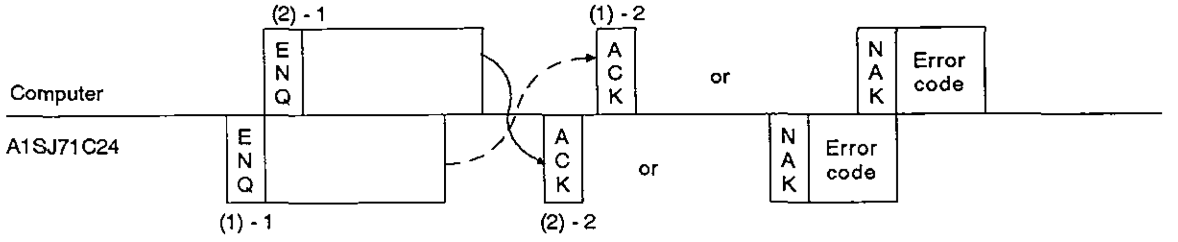
POINT

In bidirectional communications, check sum and error codes are all binary data. Note that in the dedicated protocol, they are handled in ASCII code.

10.6 Processing an A1SJ71C24 for Simultaneous Send in Full-Duplex Mode

Processing by the A1SJ71C24 varies depending on the setting (valid/invalid setting at simultaneous transmission) when the computer and the A1SJ71C24 transmit data at the same time to each other.

Example:



Buffer Memory Setting (Address 114H)	Setting	Processing by A1SJ71C24	
		Send Processing	Receive Processing
0000H	Send data : Valid Received data : Valid	After completing data send ((1)-1), the A1SJ71C24 waits for response ((1)-2) while checking time-out error. Normal or abnormal send completion is confirmed by response and its status is transmitted to the sequence program via the buffer memory.	After completing data receive ((2)-1), the A1SJ71C24 transmits the response ((2)-2). The received data and receive result are transmitted to the sequence program via the buffer memory.
0100H	Send data : Invalid Received data : Valid	After completing data send ((1)-1), the A1SJ71C24 transmits the sequence program of a simultaneous transmission error (error code: 3) via the buffer memory. The A1SJ71C24 does not wait for a response ((1)-2).	After completing data receive ((2)-1), the A1SJ71C24 transmits the response ((2)-2). The receive data and receive result are transmitted to the sequence program via the buffer memory.
0001H	Send data : Valid Received data : Invalid	After completing data send ((1)-1), the A1SJ71C24 waits for a response ((1)-2) while checking time-out error. Normal or abnormal send completion is confirmed by a response and its status is transmitted to the sequence program via the buffer memory.	Data receive ((2)-1) is ignored and received data is discarded. The response ((2)-2 is not transmitted. Data receive is not transmitted to the sequence program.
0101H	Send data : Invalid Received data : Invalid	After completing data send ((1)-1), the A1SJ71C24 transmits the sequence program of a simultaneous transmission error (error code: 3) via the buffer memory. The A1SJ71C24 does not wait for a response ((1)-2).	Data receive ((2)-1) is ignored and received data is discarded. The response ((2)-2 is not transmitted. Data receive is not transmitted to the sequence program.

POINT

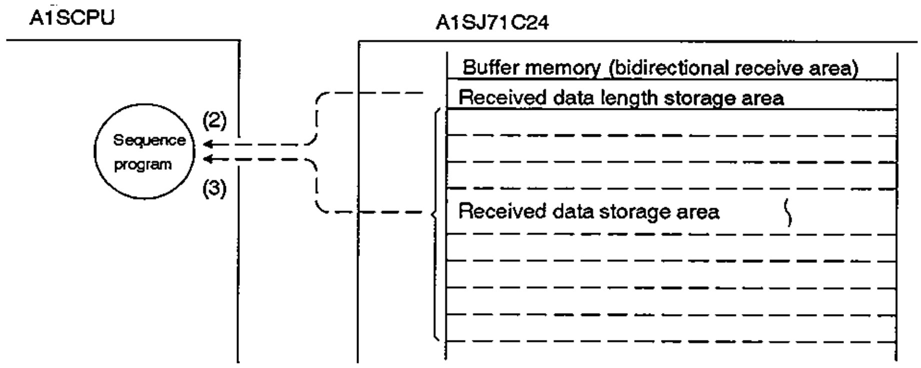
If data send of the communicating node is interrupted by sending a DC3 during simultaneous send, subsequent processing is executed according to the setting at buffer address 114H for "Simultaneous send data valid/invalid".

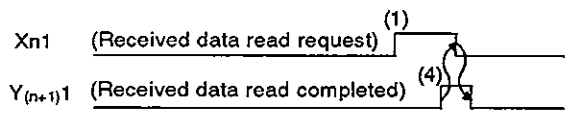
10.7 Basic Program to Read/Write Buffer Memory

The following describes a basic sequence program to bidirectional read and write data to and from the A1SJ71C24 buffer memory.

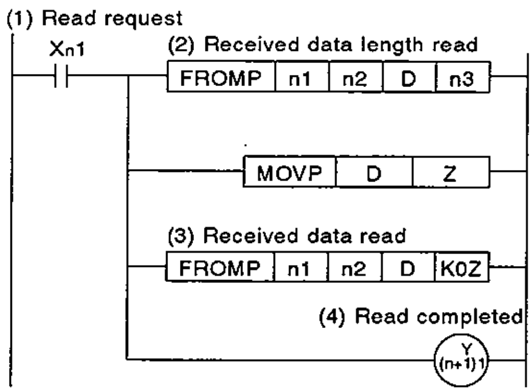
(1) Reading data from the receive area (FROM, FROMP, DFRO, DFROP)

Data is read from the buffer memory bidirectional receive area (default: 80H to FFH).





Format



Reads the received data length from the no-protocol received data length storage area of buffer memory when the read request signal (Xn1) is turned ON.

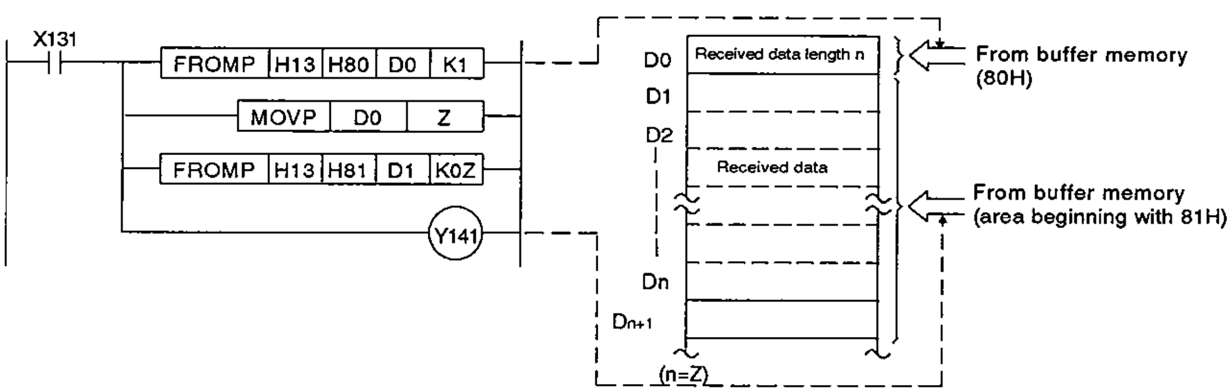
Stores the read data length to the index register (Z).

Reads the received data of the read received data length from the received data storage area of buffer memory.

Turns ON the read completed signal (Y(n+1)1) after the recieved data has been read

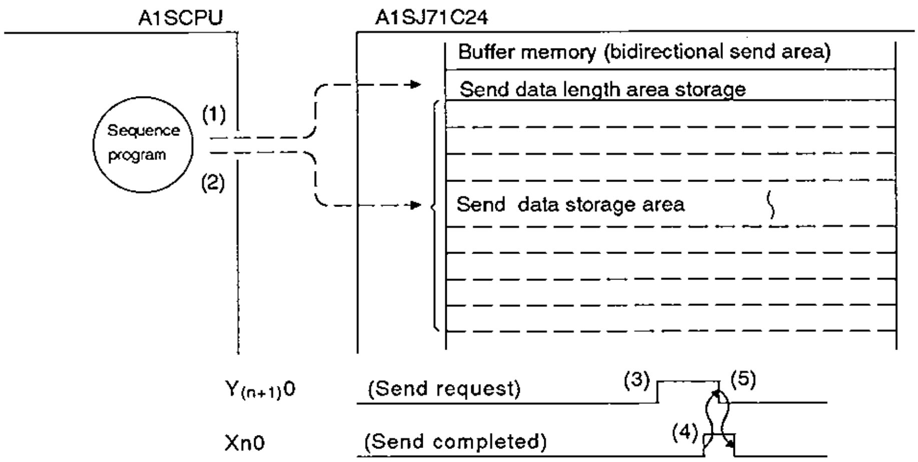
* Data read by program (3) is processed as the recieved data.

Example: To read the data of (n+1) words from the area, beginning with buffer memory address 80H, to the area beginning with D0 when the A1SJ71C24 I/O numbers are allocated to 130 to 14F (unit: word).

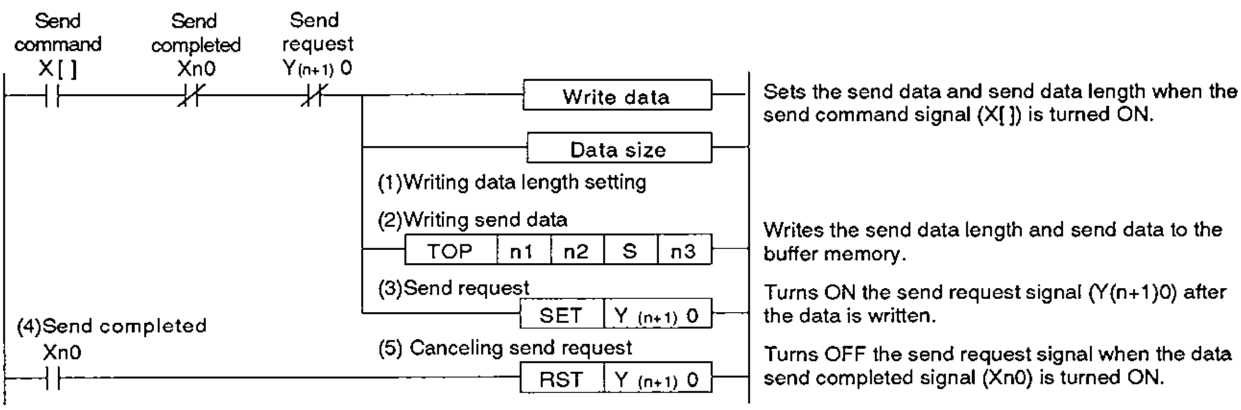


(2) Writing data to the send area (TO, TOP, DTO, DTOP)

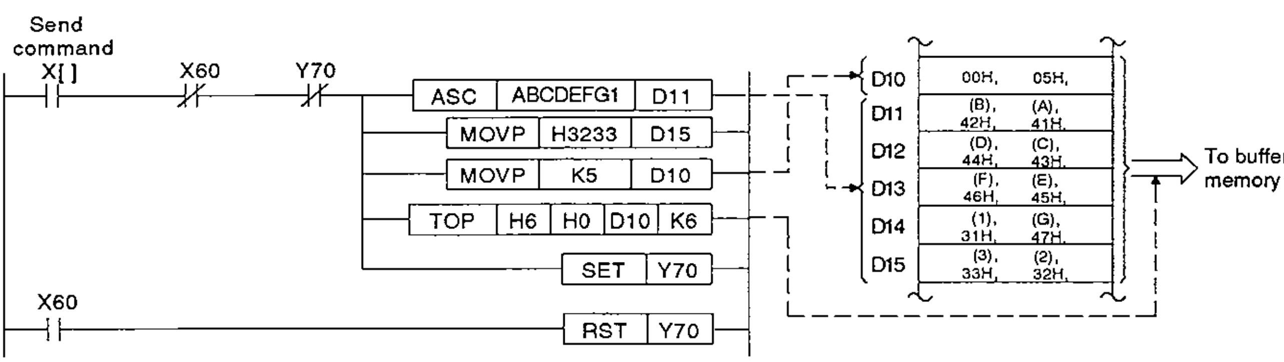
Data written to the bidirectional send area (default: 0H to 7FH).



Format



Example: To transmit 5-word data after writing "ABCDEFG123" to the buffer memory area from 1H when the A1SJ71C24 I/O numbers are allocated to 60 to 7F.



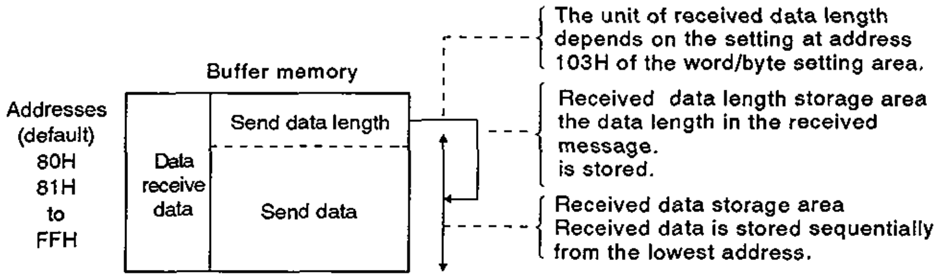
10.8 Receiving Data in the Bidirectional Mode (Computer → A1SJ71C24)

(1) Data receive area

The A1SJ71C24 stores the received data length and the received data in the data receive area.

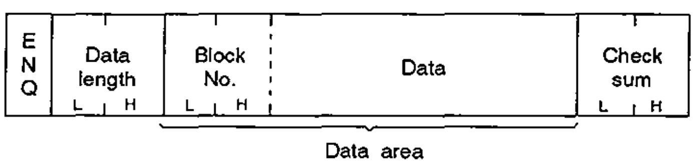
With a default setting, 80H to FFH in the buffer memory is allocated as the data receive area.

This area may be changed as needed. Section 7.4.5 gives procedure for changing the data receive area.



If the length of the data area in the message transmitted from the computer is greater than the received data storage area (default: 127 words), split the data area into several blocks so that its length is smaller than the received data storage area and append the block number to specify each data area block.

Message format example:



(2) Reading received data

The A1SJ71C24 makes a read request to the A1SCPU at the following timing (the timing at which the X1A1 signal in the program example in (4) is turned on).

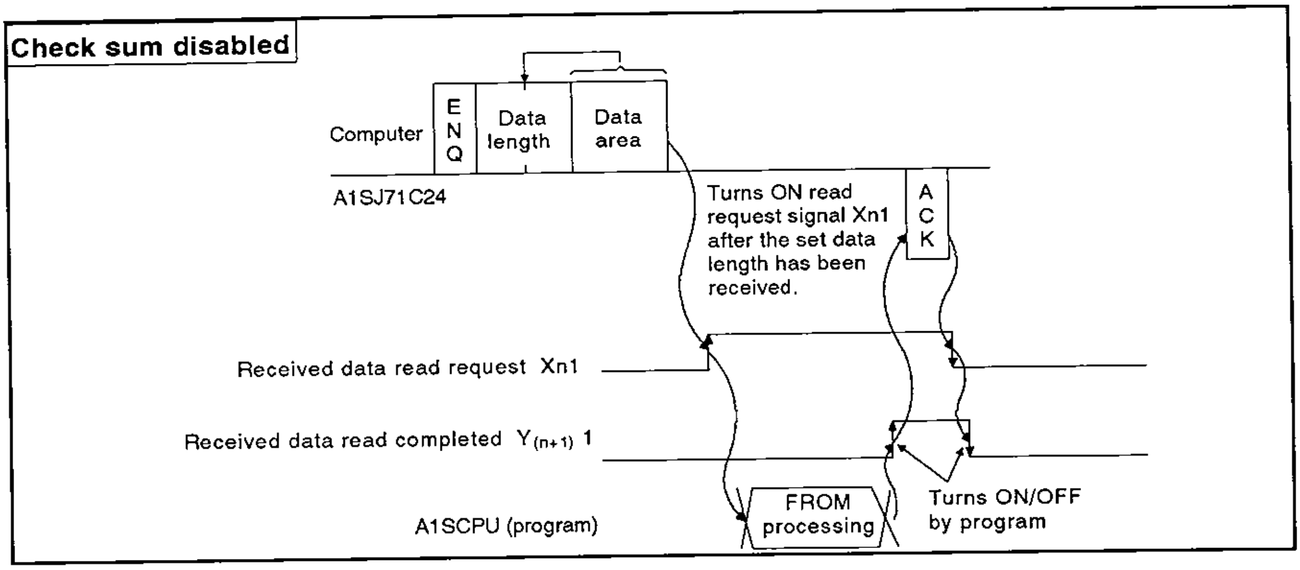
- When the data length in the message and the set data length (bytes or words as set in address 103H) have been received.
- If the check sum is processed, when the check sum has been received with the above mentioned data area.

Example:

Word/byte setting: Word units
Data length in message: 10
In this case, the A1SJ71C24 makes a read request to the the sequence program at the time 10 words of data (plus the check sum) have been received.

When the read request (Xn1) for the received data is made read the data length and that length of data with a FROM instruction in a sequence program and turn OFF the received data read completed signal (Y (n+1)1).

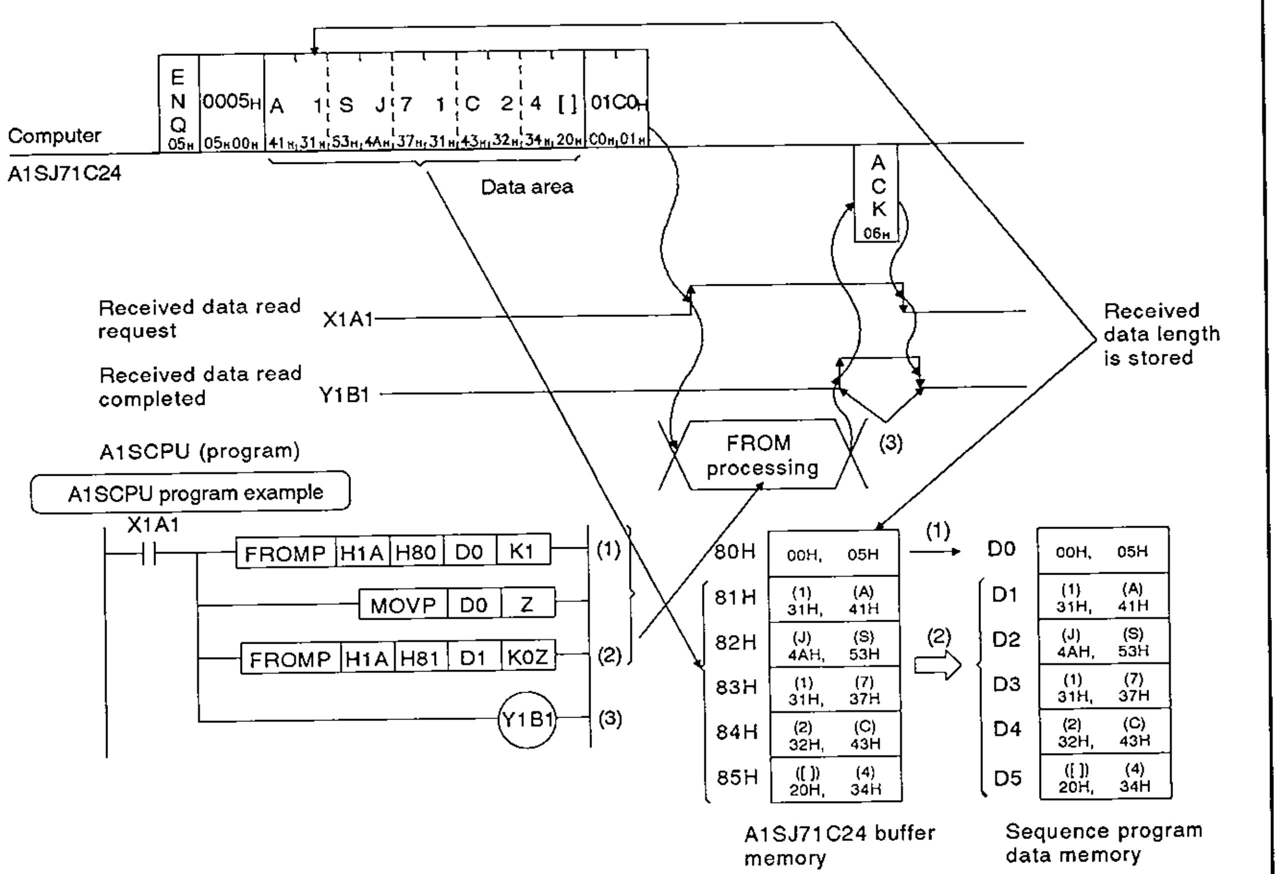
(3) Data receive processing



(4) Data receive program examples

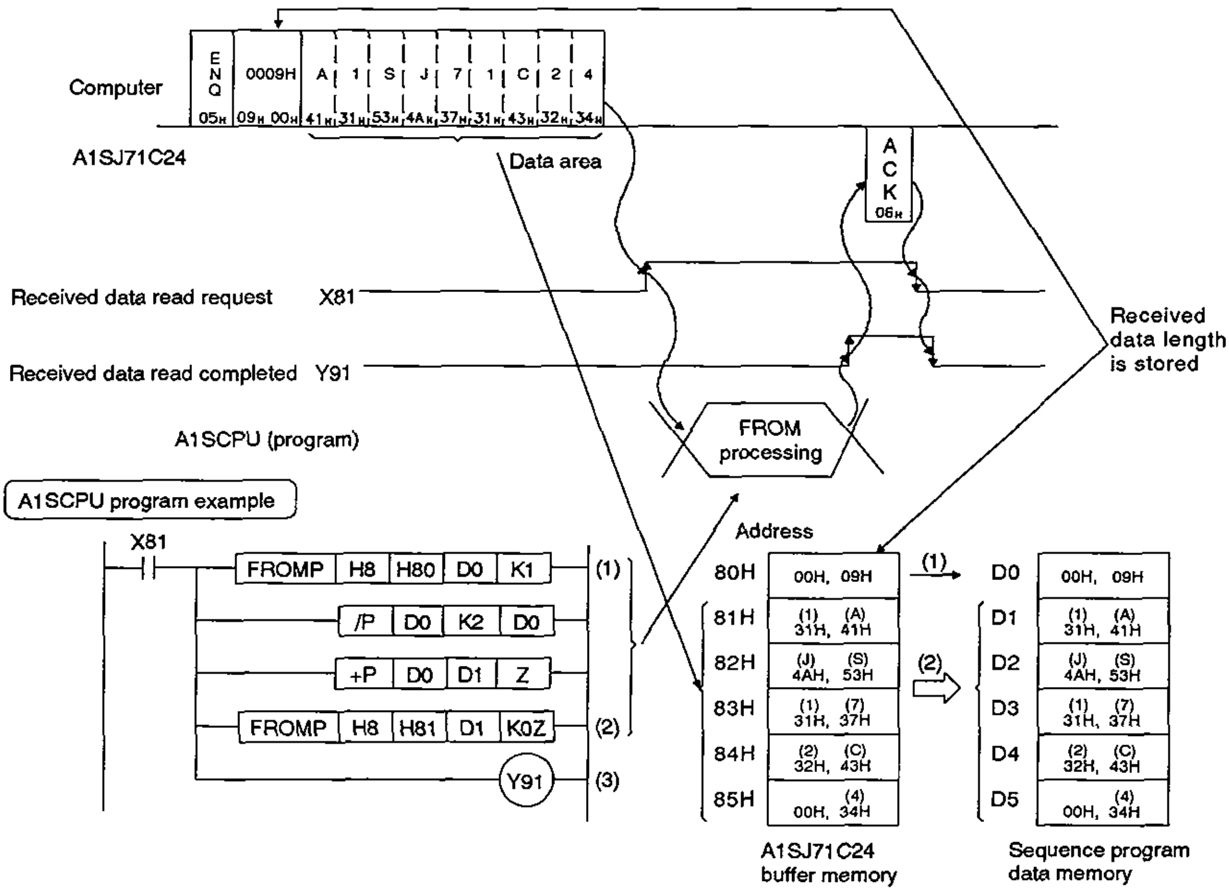
Example 1 Check sum enabled, in word units (buffer memory area allocation: default)

To store "A1SJ71C24 [ ]", received from a computer, to D0 to D5 of a A1SCPU.
(A1SJ71C24 I/O address: 1A0 to 1BF)



Example 2 Check sum disabled, in byte units (receive memory area allocation: default)

To store "A1SJ71C24", received from a computer, to D0 to D4 of a A1SCPU. (A1SJ71C24 I/O address: 80 to 9F)



POINTS

- Even if send data units are set to byte units, the FROM instruction in a sequence program operates in word units. Therefore, the received data length must be converted to the number of buffer memory points (word units).
  In the above example, 9 bytes of data must be converted into 5 words (9 ÷ 2 = 4.5 ... 5).
- When an odd number of bytes of data is received, the higher 8 bits of the last address read by the FROM instruction are "00H".

10.9 Transmitting Data in the Bidirectional Mode (A1SJ71C24 → Computer)

Transmitting means outputting data which was written to the bidirectional mode send buffer memory area (hereafter referred to as the send area), from the A1SJ71C24 to a computer in response to turning ON the A1SCPU send request signal (Y(n+1)0).

(1) Send area and writing send data

The send data length and send data are written to the send area.

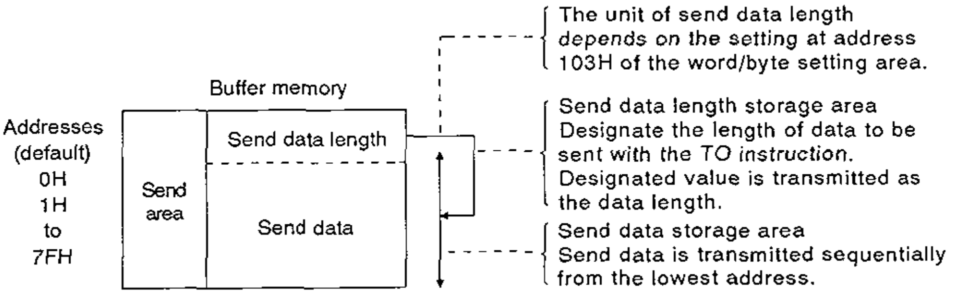
(a) The length of data to be written (having been written) to the bidirectional send data length storage area in either words or bytes.

(b) The data to be transmitted is written to the send data storage area.

When the send request signal (Y(n+1)0) is turned ON after (a) and (b) have been executed, the A1SJ71C24 transmits the designated length of designated data from the send data storage area sequentially from the lower address.

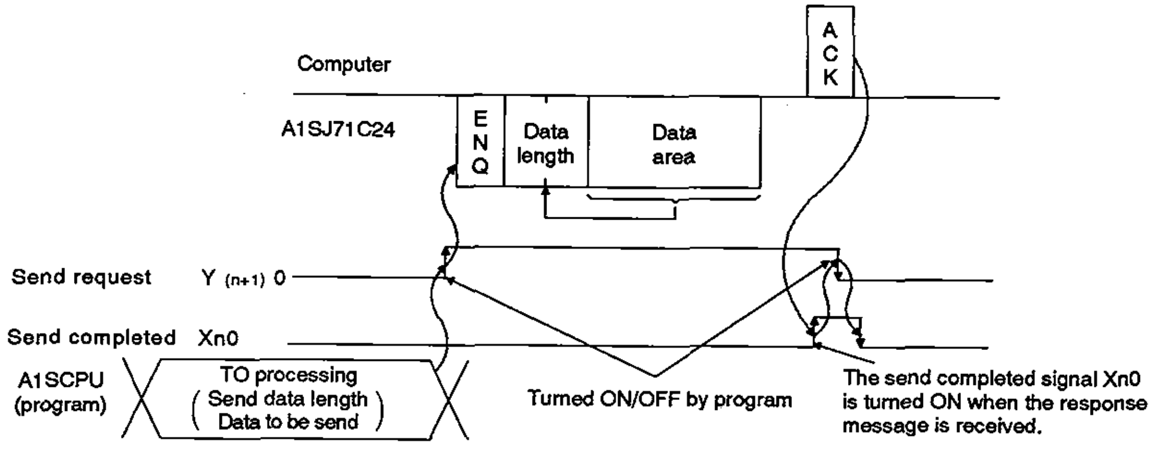
By default, the buffer memory area 0H to 7FH is allocated to the send area.

This area may be changed as needed. Section 7.4.4 gives the procedure for changing the send area addresses.



(2) Data transmitting procedure

Procedure (Check sum disabled)



POINTS

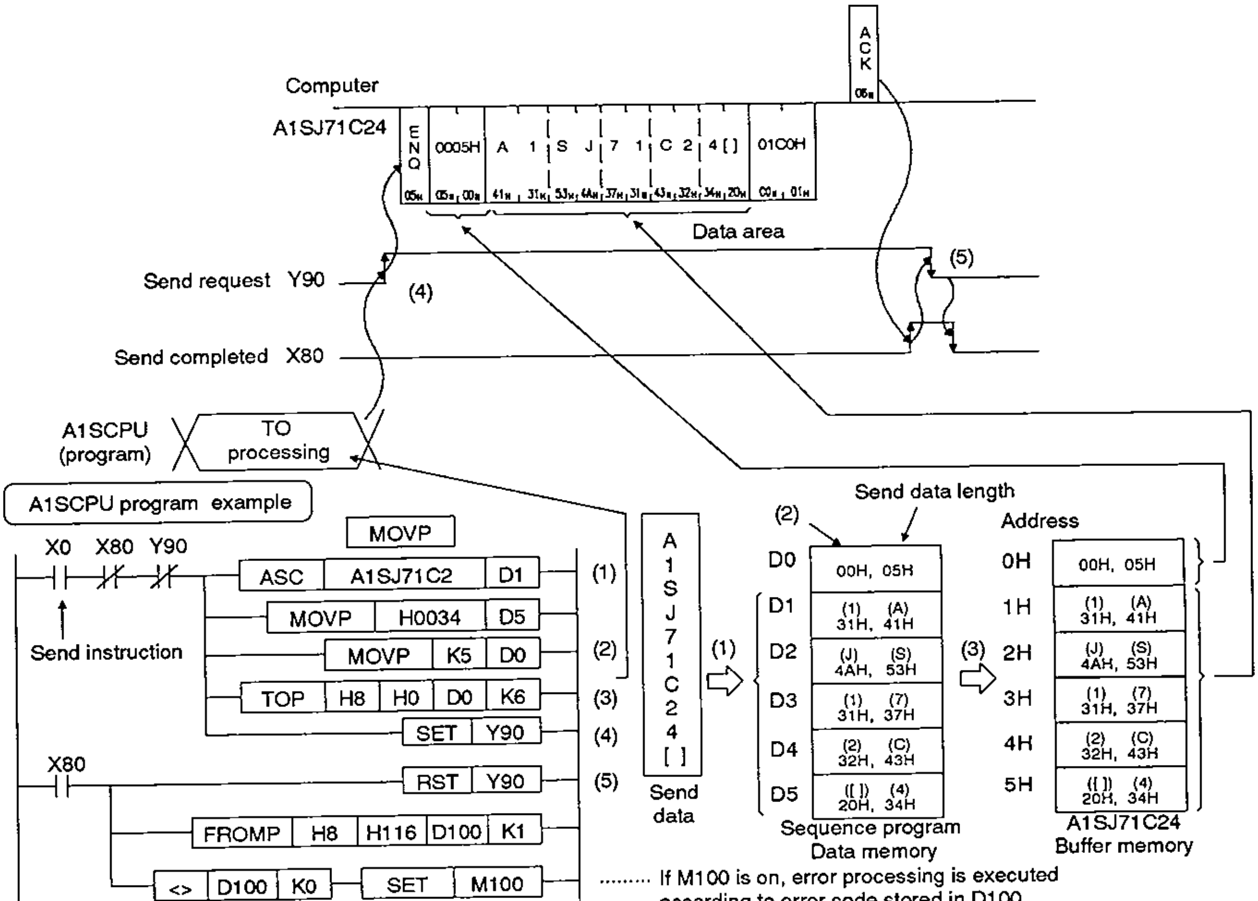
(1) An error occurs if the send data length is (a) greater than the send area, or (b) equal to "0". In this case, "1" is written as send error information to the most significant bit (bit 15) of address 116H (data send error storage area) in the special applications memory area (see Sections 10.2 and 11.2).

(2) The send data length written to the head address is transmitted as the data length.

(3) Transmission program examples

Example 1 Check sum enabled, in word units (buffer memory area allocation: default)

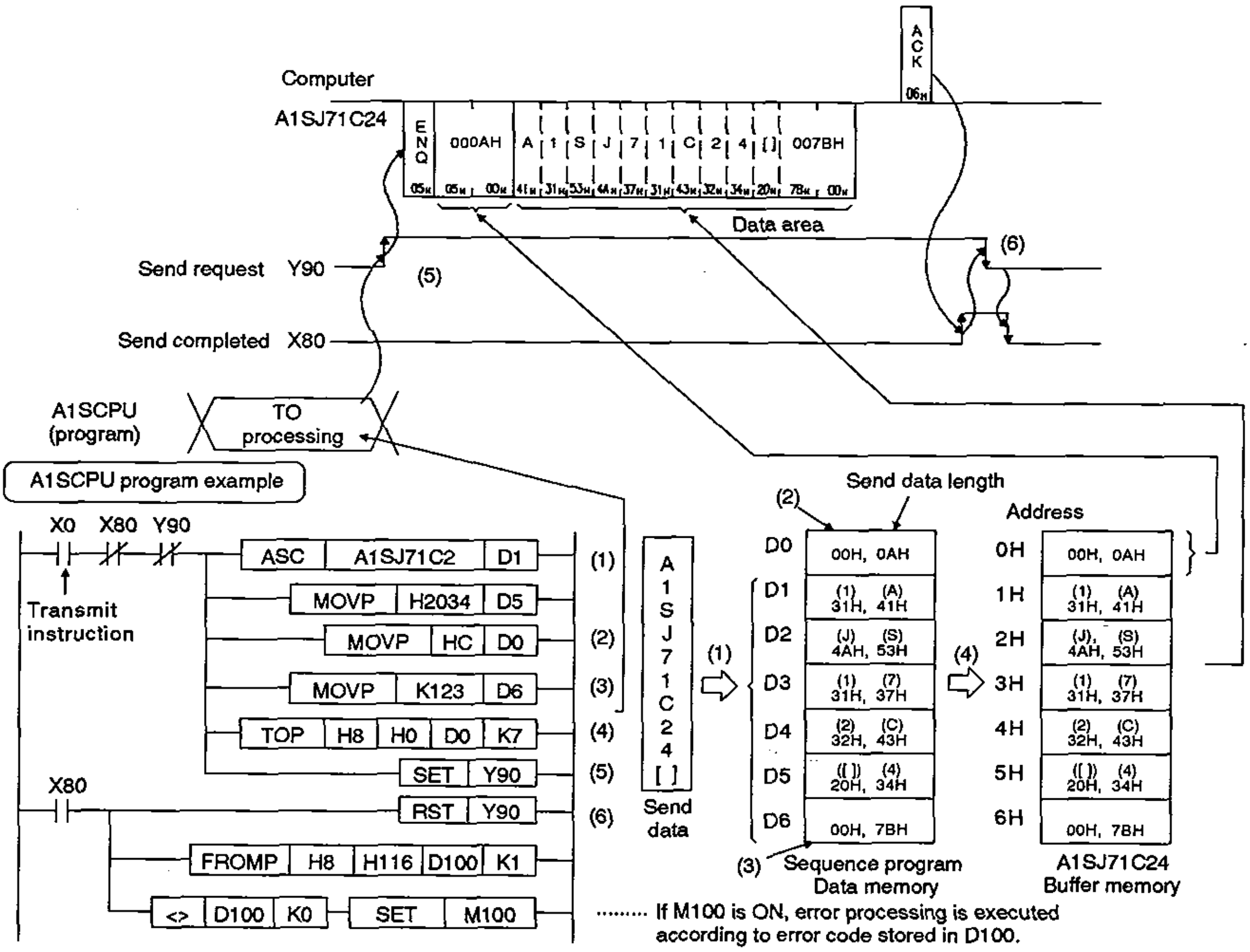
To transmit "A1SJ71C24 [ ]" from the A1SCPU to a computer after writing it to buffer memory. (A1SJ71C24 I/O address: 80 to 9F)



.... If M100 is on, error processing is executed according to error code stored in D100.

Example 2 Check sum disabled, in byte units (send data area allocation: default)

To transmit character data "A1SJ71C24 [ ]" and integer data "123" (decimal) from the A1SCPU to a computer after writing it to buffer memory. (A1SJ71C24 I/O address: 80 to 9F)



POINT

- Even if send data units are set to byte units, the TO instruction in a sequence program operates in word units. Therefore, the length of send data differs from the data length designated by the TO instruction.

[PRINTER FUNCTIONS]

This section describes the registration, reading, and output of messages when the printer functions are used with the A1SJ71C24-PRF.

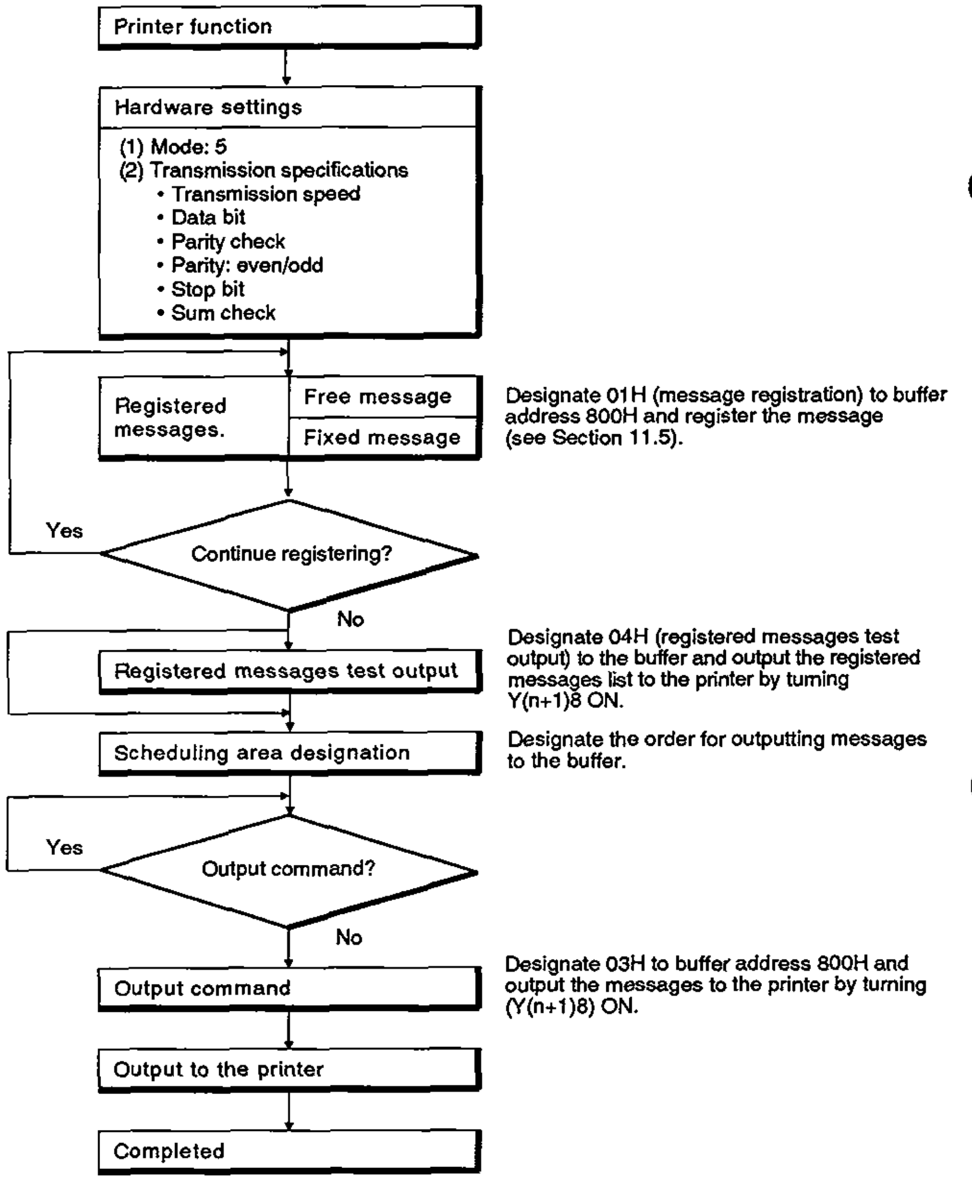
11. PRINTER FUNCTIONS

This section explains the procedures for using a printer function to output data from a computer or PC CPU to a printer.

Read this section when using the printer function. It is not necessary to read this section when only the computer link function is used.

11.1 Procedure for Using the Printer Function

The following flowchart explains the procedure for using the printer function.



POINT

Section 4.5.2 gives details about connecting to a printer.

11.2 Precautions Before Programming

This section gives the precautions to take before starting the programming to use a printer function.

11.2.1 Free messages and fixed messages

Free messages, registered in the buffer, contain variable data (such as data in a data register).

Fixed messages, registered in the EEPROM, contain fixed data (such as table frames and model names).

- Creating a table: example

Register the table frame and model as fixed messages.

Model	Check Results
A1SJ71C24-R2	
A2ACPU	

Then, register the check results as free messages.

O.K
Fault

For example, the following table can be created by using fixed messages and free messages.

Model	Check Results
A1SJ71C24-R2	O.K
A2ACPU	Fault

11.2.2 Precautions when using a printer function

(1) Turning OFF the printer after connecting the A1SJ71C24-PRF to a printer

Turning OFF the printer after connecting the A1SJ71C24-PRF to the printer during a parity check will cause a parity error.

(2) CD terminal checked/not checked designation

CD terminal checked/not checked designation must be done in accordance with the printer specifications (see Section 7.1).

11.2.3 Writing to the special-applications area of the buffer (including printer function areas)

The following precautions must be taken when writing to the special-applications area (including the printer function areas) of the A1SJ71C24-PRF buffer:

(1) Since the buffer is not backed up by a battery, all data in the buffer is returned to default values when the CPU is turned ON, reset, or the operating mode is changed.

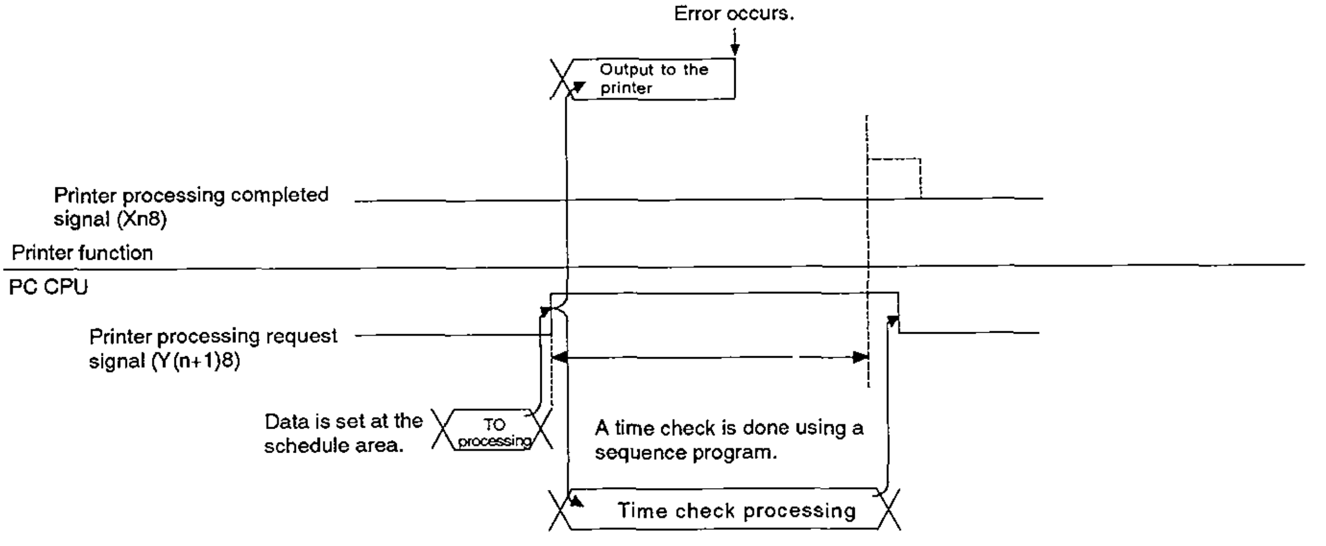
Setting data or updating data must be written to the buffer every time the CPU is turned ON, reset, or the operating mode is changed.

(2) Data can be written to the special-applications area (100H to 11FH) excluding the mode switching area only by using a TO instruction in a sequence program.

11.2.4 Printer Errors

When outputting messages to the printer, if (a) an error occurs, or (b) the printer is not connected, the printer processing completed signal (Xn8) will not go ON.

Therefore, it is necessary to do a time check using a sequence program.

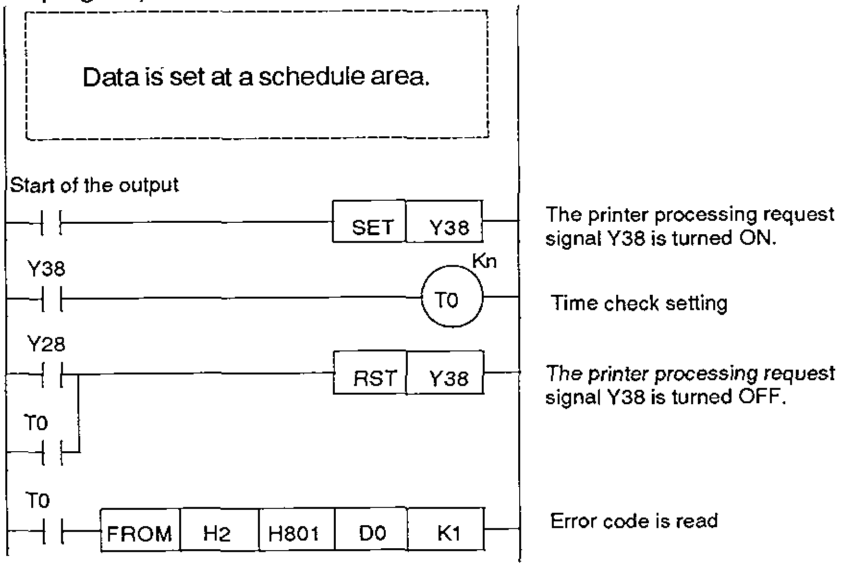


After the printer processing request signal (Y(n+1)8) goes ON, continue the time check until the printer processing completed signal (Xn8) is turned ON.

If an error occurs when a message is being output, the printer processing request signal (Y(n+1)8) goes OFF.

To detect a printer error, add a sequence program as shown below.

(Sequence program) A1SJ71C24-PRF I/O addresses: 20 to 3FH



POINT

Set the value of a time check according to the time it takes the printer to print one character.

11.3 Designating the Buffer Memory to Use Printer Functions and Reading

The buffer of the A1SJ71C24-PRF has a message registration area (address 800H to DFFH) to set the information that is output to the printer (see Section 3.5).

This section explains the designation method and gives examples showing how to set and change a setting in the message registration area of the buffer.

11.3.1 Designating the message function designation area

A message registration, read, output, test output, or printer test can be set in the message function designation area.

Designation method

b15 to b8 b7 to b0

800H (Default: 0)

Write any from 0 to 5.
0: Printer function not designated
1: Message registration
2: Message read
3: Message output
4: Test output of a registered message
5: Printer test

POINT

The eight bits of b8 to b15 at buffer address 800H can be set to 0 or 1 (the A1SJ71C24-PRF ignores the setting).

Designation example

To register a message (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

(Sequence program)

```
|--| |--[ TOP | H2 | H800 | K1 | K1 ]--|
```

"1" is written to buffer address 800H.

11.3.2 Designating the schedule area

The schedule area is used to set the information that is output to the printer.

The schedule area is configured as follows:

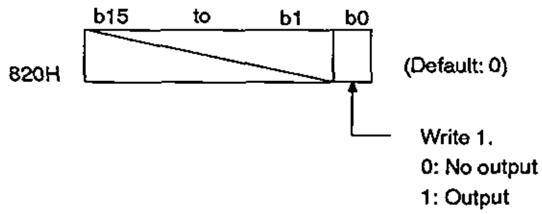
Buffer		Reference
820H	Output CR/LF designation	....(1)
821H	Output pointer designation	....(2)
822H	Number of outputs designation	....(3)
823H	Output number 1st	.....(4)
824H	Output number 2nd	
to		
887H	Output number 100th	
888H to 89FH	Unusable	

(1) to (4) on the following pages give details about each setting.

(1) Output CR/LF designation

This designates whether or not a CR/LF is output if a CR/LF could not be detected in 80 characters.

Designation method



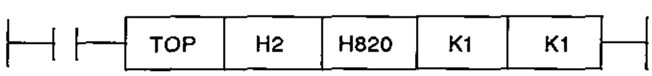
POINT

If 79 characters and a CR/LF are output, add a space to the 79 characters to make 80 characters, and set the designation of the output CR/LF to output ("1").

Designation example

To output a CR/LF (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

(Sequence program)

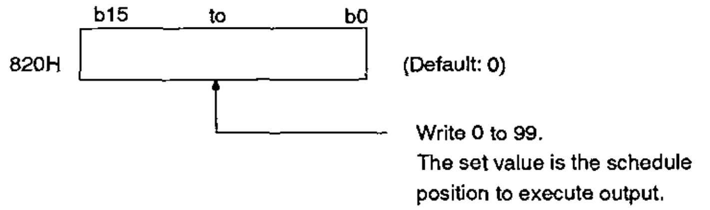


"1" is written to buffer address 820H.

(2) Output pointer designation

The following explains the designation method and gives an example showing how to execute output from a designated schedule position to the printer.

Designation method



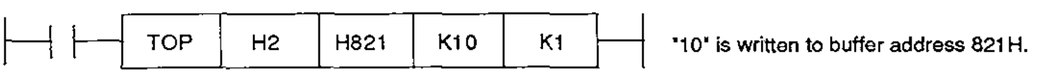
POINT

An error will occur if the sum of the number of output pointers and the number of outputs exceeds 100.

Designation example

To output data from the 10th schedule area to the printer (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

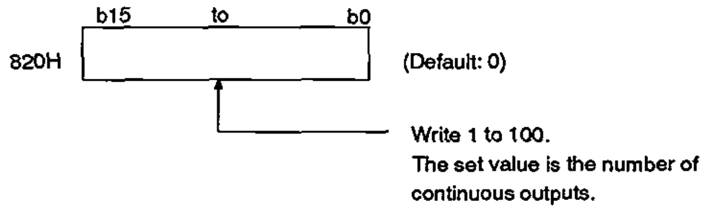
(Sequence program)



(3) Designating the number of outputs

The following explains the method and gives an example of the designation of the number of pieces of output data that is continuously output from the schedule position designated by setting an output pointer.

Designation method



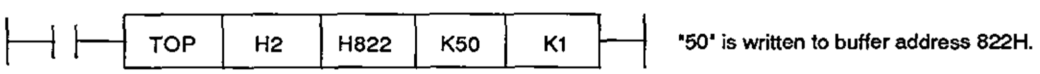
POINT

An error will occur if the sum of the number of output pointers and the number of outputs exceeds 100.

Designation example

To output data from the 10th schedule area to the printer (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

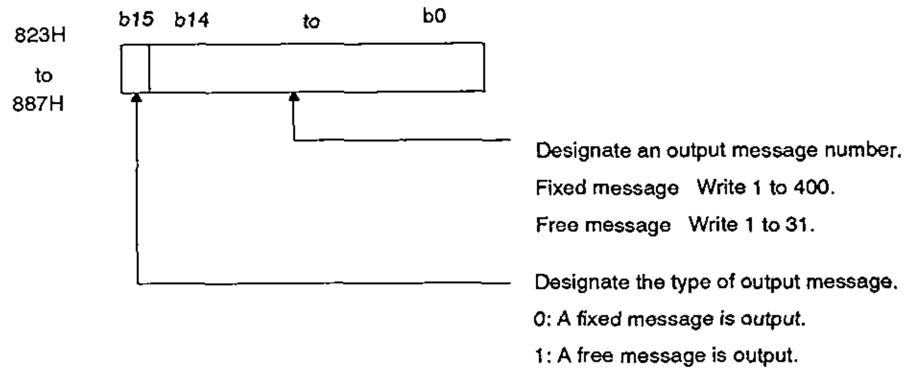
(Sequence program)



(4) Designation of an output number

The following explains the method and gives an example of the designation of the message number that is output to the printer.

Designation method



Designation example

To set the fixed message numbers 1 to 5 and the free message numbers 11 to 15 (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

(Sequence program)

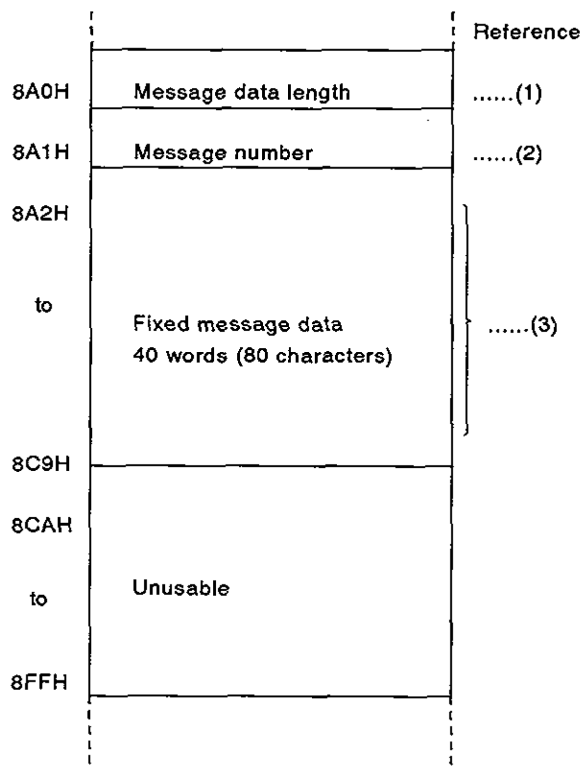
TOP	H2	H823	H1	K1	Designates an output of fixed message number 1.
TOP	H2	H824	H2	K1	Designates an output of fixed message number 2.
TOP	H2	H825	H800B	K1	Designates an output of free message number 11.
TOP	H2	H826	H3	K1	Designates an output of fixed message number 3.
TOP	H2	H827	H800C	K1	Designates an output of free message number 12.
TOP	H2	H828	H800D	K1	Designates an output of free message number 13.
TOP	H2	H829	H800E	K1	Designates an output of free message number 14.
TOP	H2	H830	H4	K1	Designates an output of fixed message number 4.
TOP	H2	H831	H5	K1	Designates an output of fixed message number 5.
TOP	H2	H832	H800F	K1	Designates an output of free message number 15.

11.3.3 Designating the fixed message access area (only a sequence program can be used for this setting)

The following explains the method and gives an example showing the designation of the fixed message access area used for registering fixed messages.

The fixed message access area is configured as follows:

Buffer (fixed message access area)



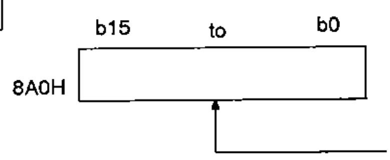
POINT

- A message is written to the EEPROM when Y(n+1)8 goes ON.
- Messages can be written to the EEPROM up to 100,000 times per area.

(1) Designating the message data length

The following explains the method and gives an example showing the designation of a message data length.

Designation method



Write the number of characters of the fixed message to be registered.

POINT

Set the message data length in the following range:

- 0 <number of characters ≤ 80

Designation example

To set a fixed message length at 14 characters (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

(Sequence program)

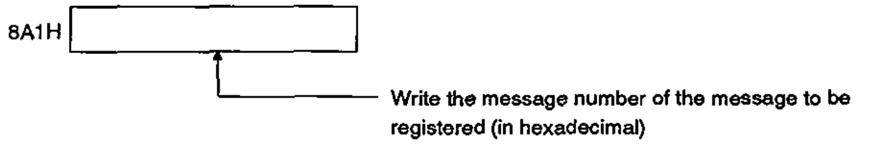
TOP	H2	H8A0	K14	K1

"14" is written to buffer address 8A0H.

(2) Designating a message number

The following explains the method and gives an example showing the designation of a message number to register a fixed message.

Designation method



POINT

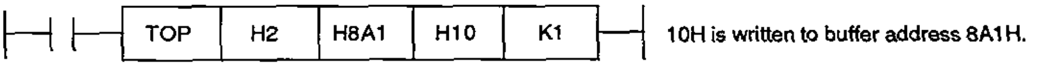
Set the message number in the following range:

- 1 ≤ message number ≤ 400

Designation example

To register a fixed message with message number 16 (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

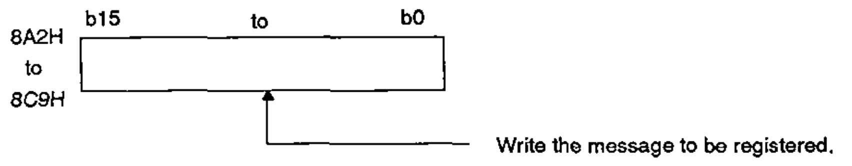
(Sequence program)



(3) Designating fixed message data

The following explains the method and gives an example showing the designation of fixed message data.

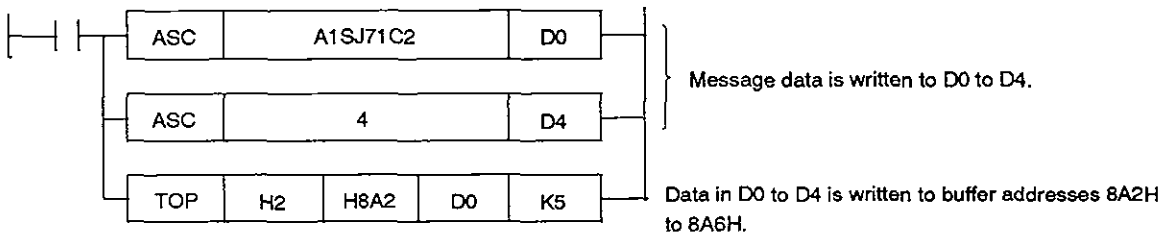
Designation method



Designation example

To register fixed message data "A1SJ71C24" (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

(Sequence program)

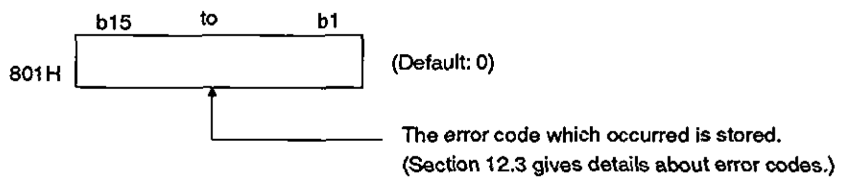


11.4 Reading from the special-applications area of the buffer

11.4.1 Reading from the message error storage area

The following explains the error contents stored in the message error storage area and gives a reading example.

Designation method



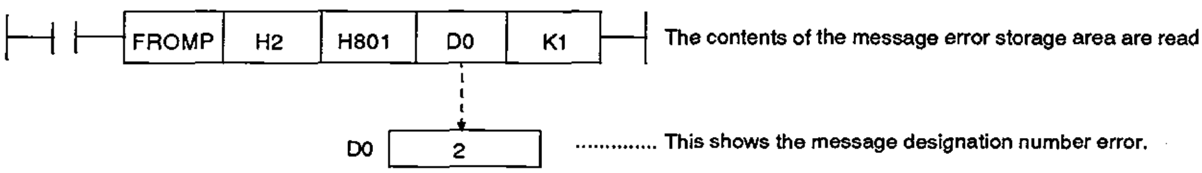
POINT

When several errors occur, the error code of the error that occurred first is stored.

Designation example

To read the contents of the message error storage area (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

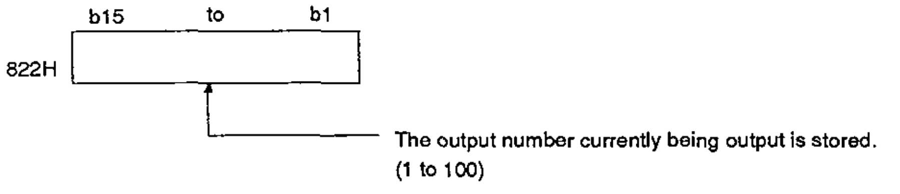
(Sequence program)



11.4.2 Reading from the output state storage area

The following explains the contents stored in the output state storage area and gives a reading example.

Designation method



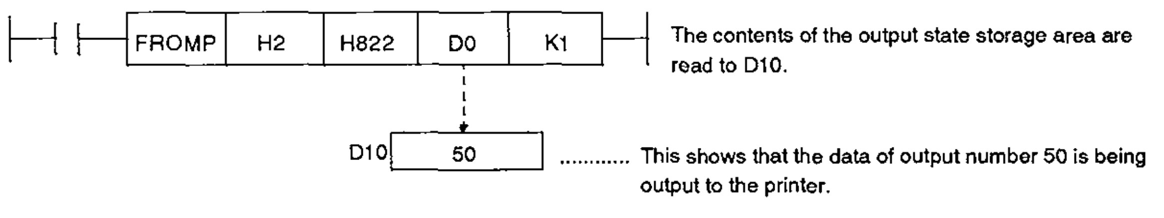
POINT

Stored contents are cleared when the printer processing completed signal (Xn8) goes ON.

Designation example

To read the contents of the output state storage area (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

(Sequence program)



11.5 Registering and Reading Messages

Messages can be registered and read by using the following methods:

(1) Registration and read of a message from a computer (fixed messages only)

A message is registered and read by using commands (CI and CJ) in dedicated protocol mode 1 to 4.

(2) Registration and read of a message from a PC CPU (free messages and fixed messages)

Messages are registered to/read from the fixed/free message areas of the buffer of a printer by using FROM and TO instructions.

11.5.1 Registering messages

(1) Registering messages from a computer

The following explains the contents and method and gives examples of the designation of a protocol to register messages from a computer.

(a) Command

Item	Command		Processing Contents	Number of Points Processed per Communications	PC CPU Status		
	Symbol	ASCII Code			During STOP	During RUN	
						SW04 ON	SW04 OFF
Message registration	CI	43H, 49H	Registration of fixed message data	40 words	O	O	O

POINT

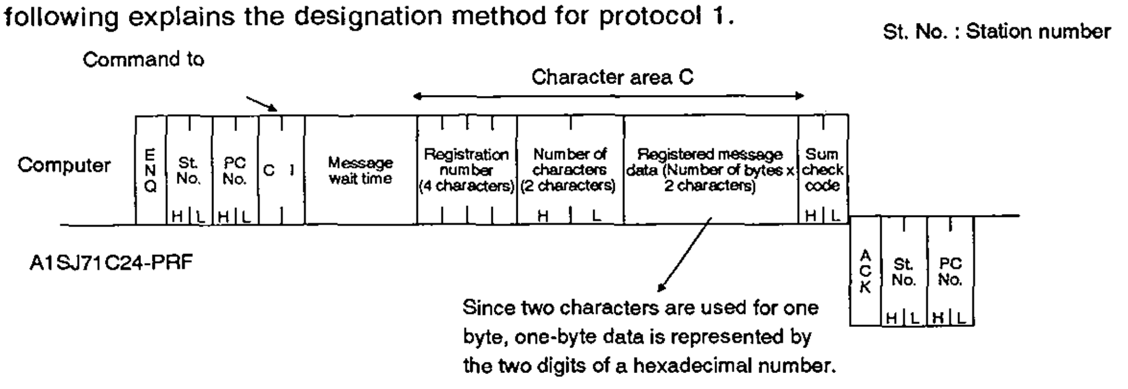
The computer link section of this manual gives details about dedicated protocol operations.

(b) Message registration (fixed messages only)

The following explains the method and gives an example showing the designation of a protocol to register a message from a computer.

Designation method

The following explains the designation method for protocol 1.



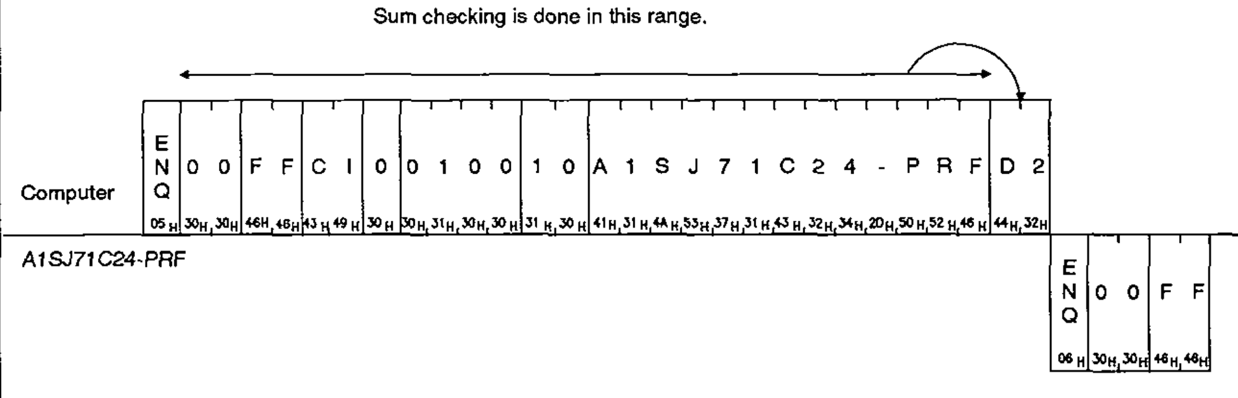
POINT

The designated range of a registration number and the number of characters must satisfy the following conditions.

- 1 ≤ registration number ≤ 400
- 1 ≤ number of characters ≤ 80

Designation example

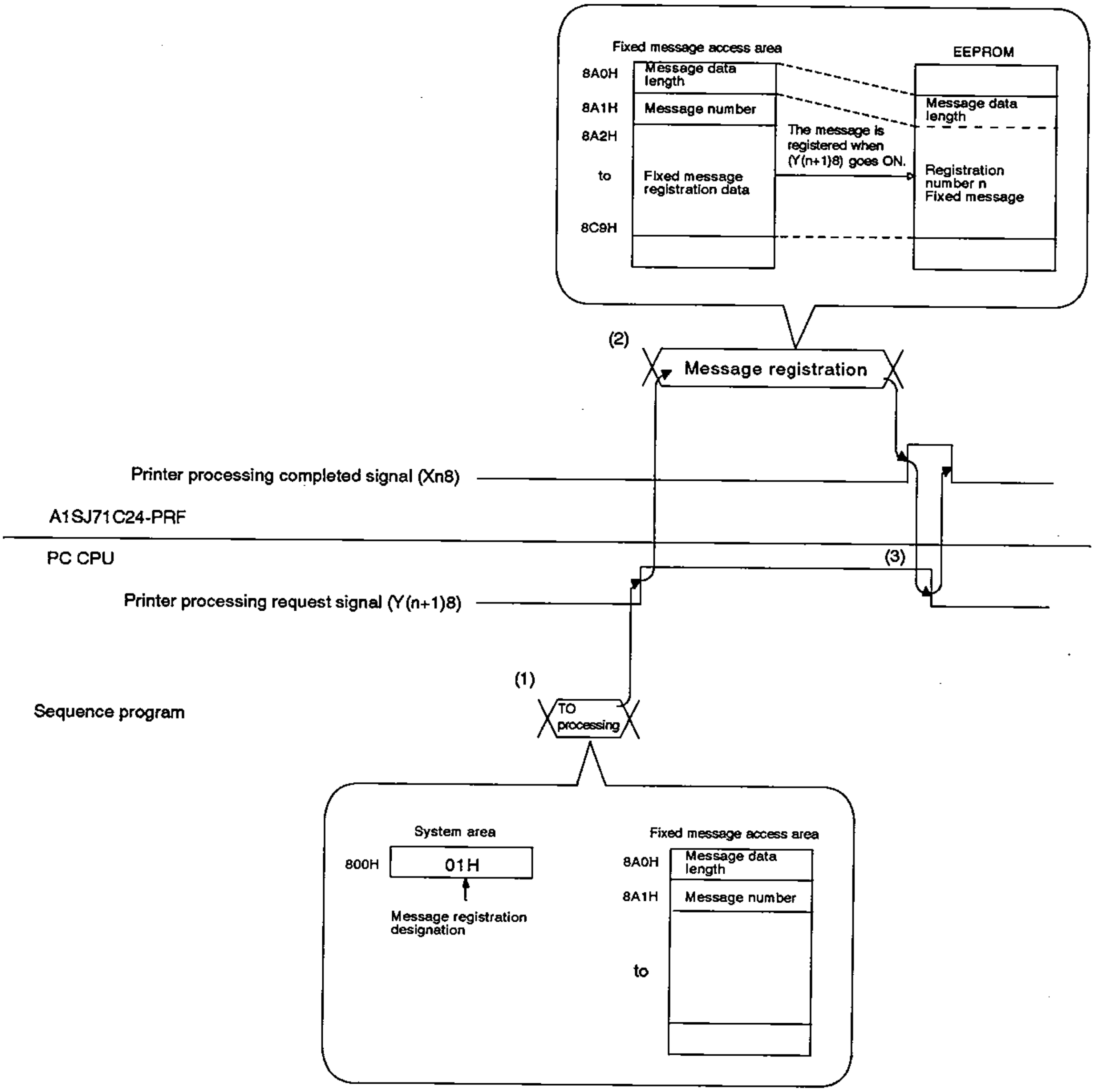
To register "A1SJ71C24-PRF" to the fixed message of registration number 100 (the message wait time is 0 msec).



(2) Registering messages from a PC CPU

The following explains the method and gives examples of registering messages from a PC CPU.

(a) Registering fixed messages



1) Designate message registration (01H) to buffer address 800H, write the message number to be registered to 8A1H, and (using a sequence program) write the message to be registered to 8A2H to 8B1H.

After writing to the buffer, turn ON the printer processing request signal (Y(n+1)8) with a sequence program.

2) When the printer processing request signal (Y(n+1)8) goes ON, the A1SJ71C24-PRF writes the message from the buffer to the EEPROM.

   The message of the designated message data length is written to the EEPROM.

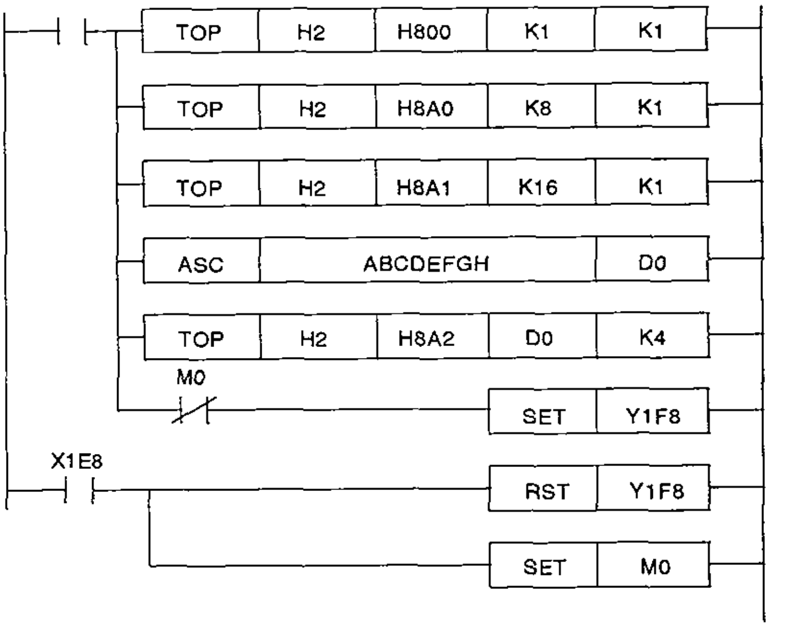
   After registration, the A1SJ71C24-PRF turns ON the printer processing completed signal (Xn8).

3) After the A1SJ71C24-PRF has turned ON the printer processing completed signal (Xn8), turn OFF the printer processing request signal (Y(n+1)8) with a sequence program.

Message registration example

i) To register "ABCDEFGH" to fixed message registration number 16 (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

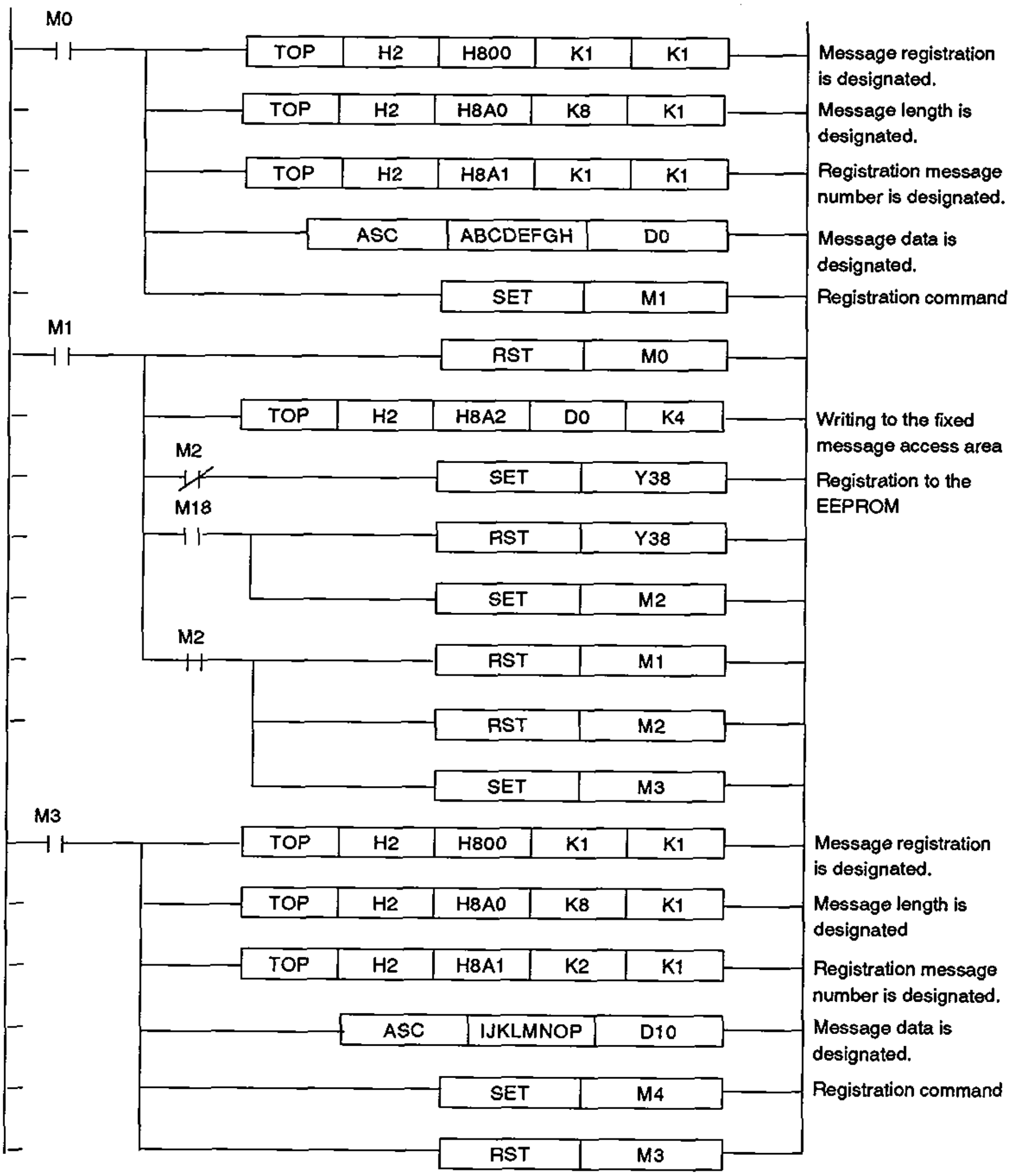
(Sequence program)

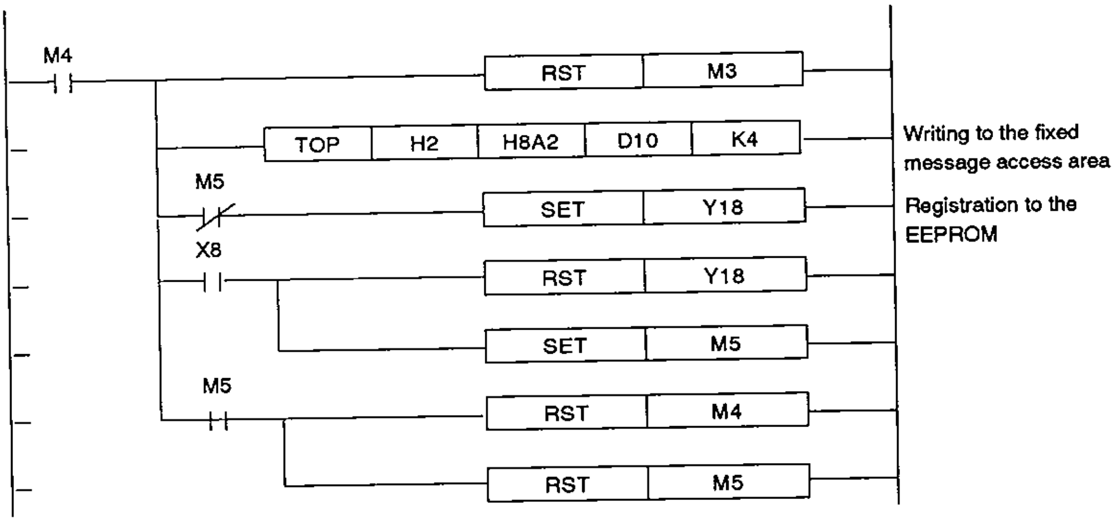


ii) To register "ABCDEFGH" to the fixed message No.1 and "IJKLMNOP" to the fixed message No.2.

(A1SJ71C24-PRF I/O addresses: 20 to 3F)

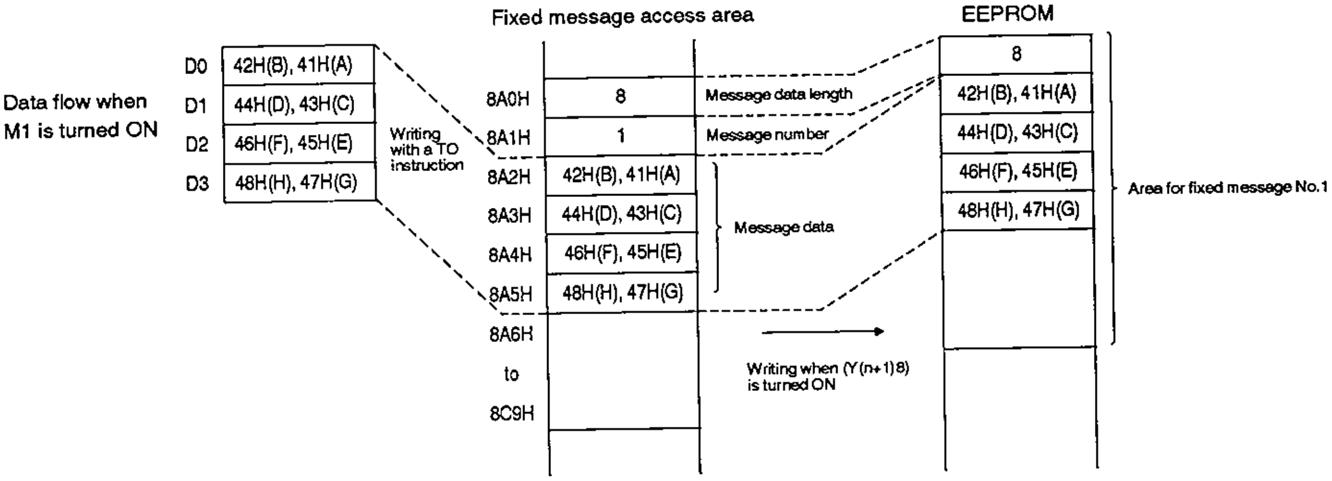
(Sequence program)



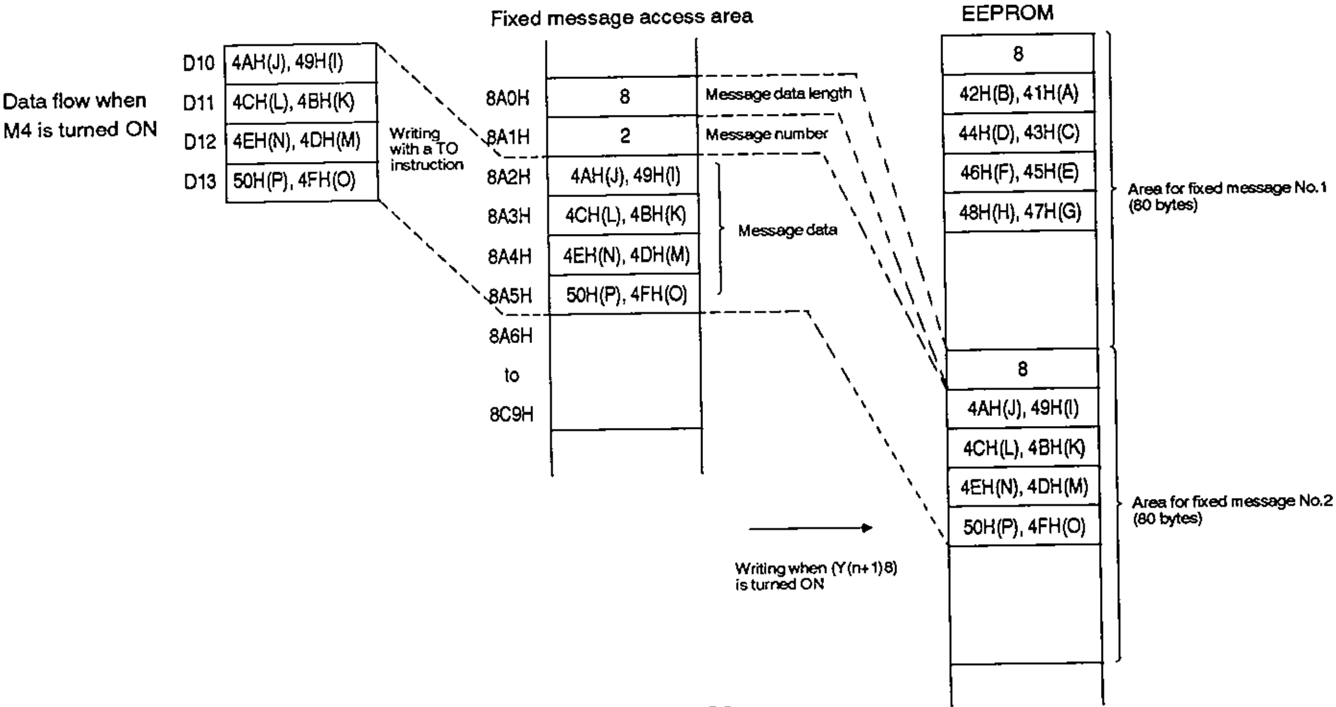


Messages of the above example are stored to the EEPROM by the following procedure:

Message 1: ABCDEFGH



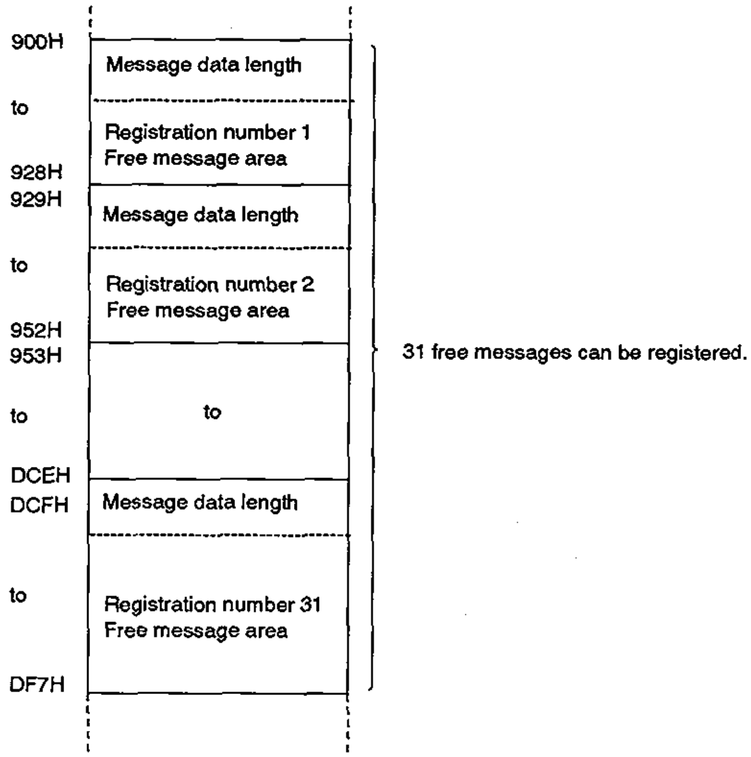
Message 2: IJKLMNOP



(b) Registering free messages

Buffer addresses 900H to DF7H are used for the free message registration area.

Buffer

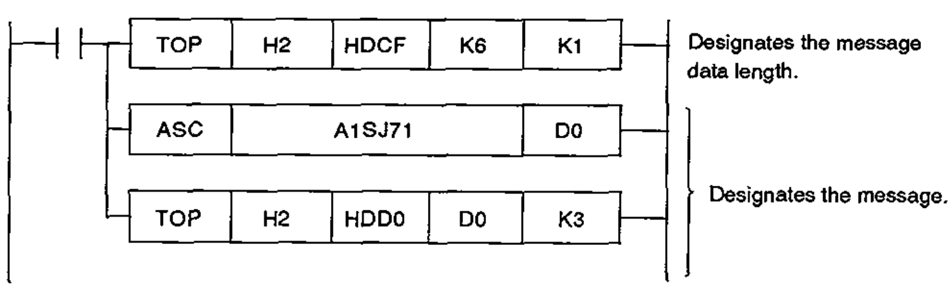


A TO instruction is used for registering a free message.

Message registration example

To register "A1SJ71" in the free message area of registration number 31 (A1SJ71C24-PRF I/O addresses: 20H to 3FH).

(Sequence program)



11.5.2 Reading messages

(1) Reading messages from the computer

The following explains the designated contents and method and gives an example of a protocol to read a message from the computer.

(a) Command

Item	Command		Processing Contents	Number of Points Processed per Communications	PC CPU Status		
					During STOP	During RUN	
	Symbol	ASCII Code				SW04 ON	SW04 OFF
Message read	CJ	43H, 4AH	Read of fixed message data	40 words	O	O	O

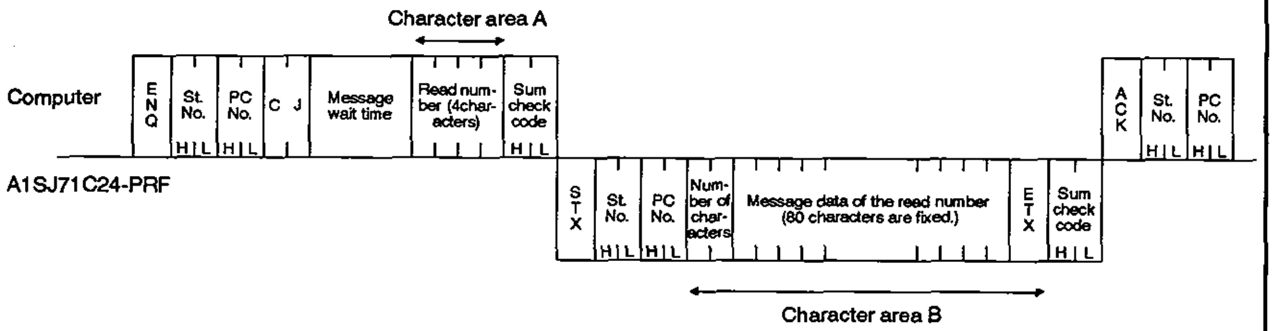
(b) Reading messages (fixed messages)

The following explains the method and gives an example showing the designation of a protocol to read a message from a computer.

Designation method

St. No. : Station number

The following explains the designation method for protocol 1.



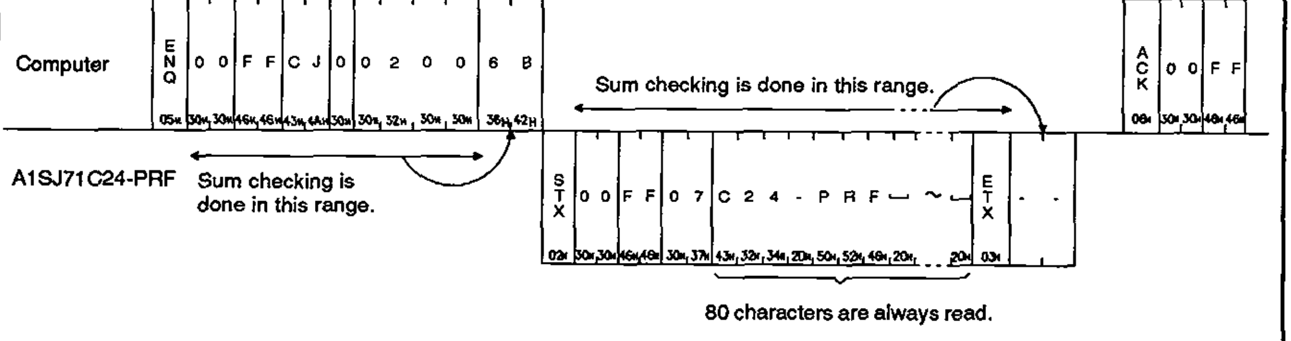
POINT

The designated range of the read number must satisfy the following condition:

- 1 ≤ read number ≤ 400

Designation example

To read the message in which "C24-PRF" of registration number 200 is registered



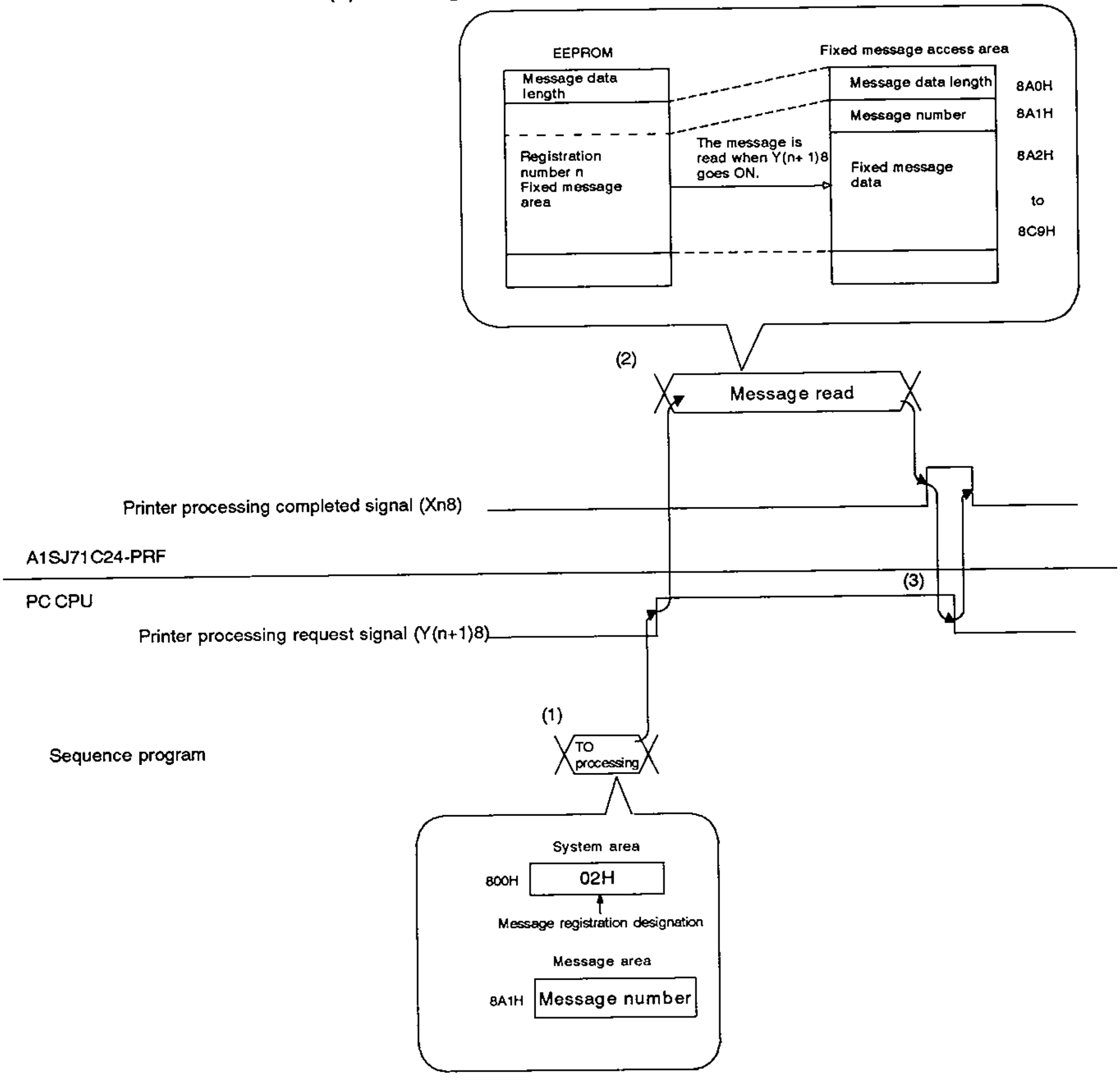
POINT

The registered message and the remaining area (a total of 80 characters) are read.

(2) Reading messages from a PC CPU

The following explains the method and gives examples of reading messages from a PC CPU.

(a) Reading fixed messages



1) Designate message read (02H) to buffer address 800H with a sequence program, and write the message number that is read to 8A1H. After writing to the buffer, use a sequence program to turn ON the printer processing request signal (Y(n+ 1)8).

2) When the printer processing request signal (Y(n+ 1)8) goes ON, the A1SJ71C24-PRF reads a message from EEPROM to a fixed message area of the buffer. After reading is executed, the A2CCPUC24-PRF turns ON the printer processing completed signal (Xn8).

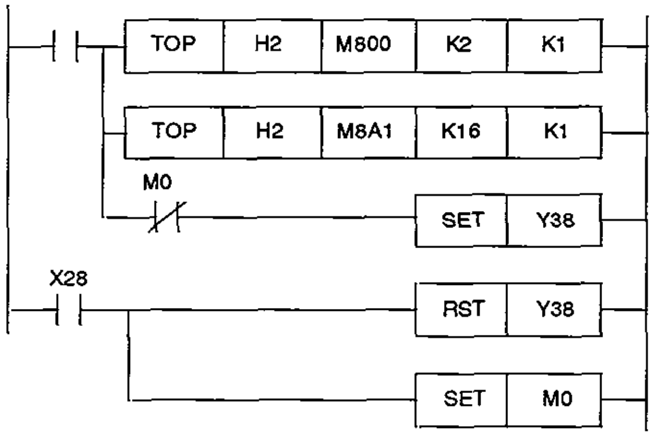
3) After the printer function has turned ON the printer processing completed signal (Xn8), turn OFF the printer processing request signal (Y(n+ 1)8) with a sequence program.

Message reading example

To read THE fixed message of registration number 16

(A1SJ71C24-PRF I/O addresses: 20H to 3FH.)

(Sequence program)



(b) Reading free messages

A FROM instruction from the buffer is used for reading free messages.

Message reading example

To read the free message registered in registration number 31 to D0 to D3 (A1SJ71C24-PRF I/O addresses: 20H to 3FH.)

(Sequence program)

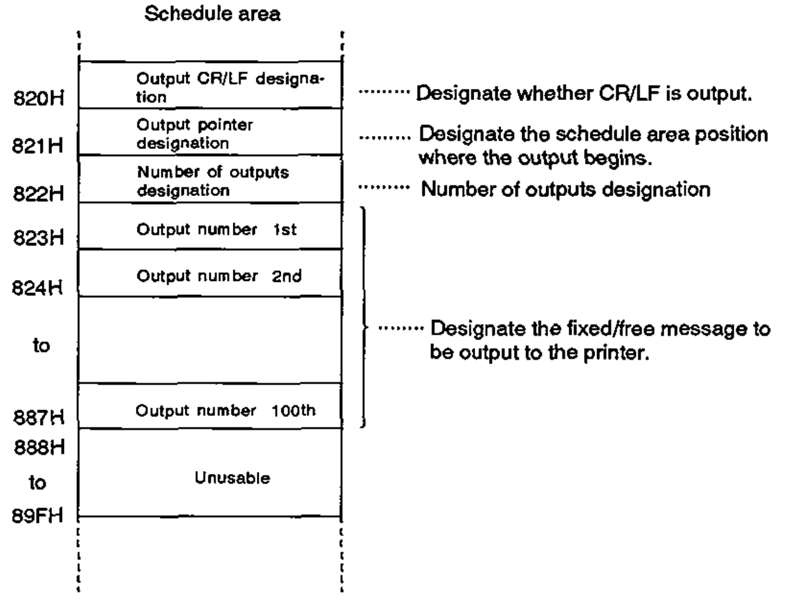
FROMP	H2	HDCF	D1	K1
FROMP	H2	HDD0	D1	K1
FROMP	H2	HDD1	D2	K1
FROMP	H2	HDD2	D3	K1

11.6 Message Output

This section explains the procedure for outputting a registered message to the printer.

11.6.1 Designating the schedule area

The message is output by designating the message output to buffer address 800H (message function designation area) and setting a fixed/free message number at a schedule area (820H to 887H).

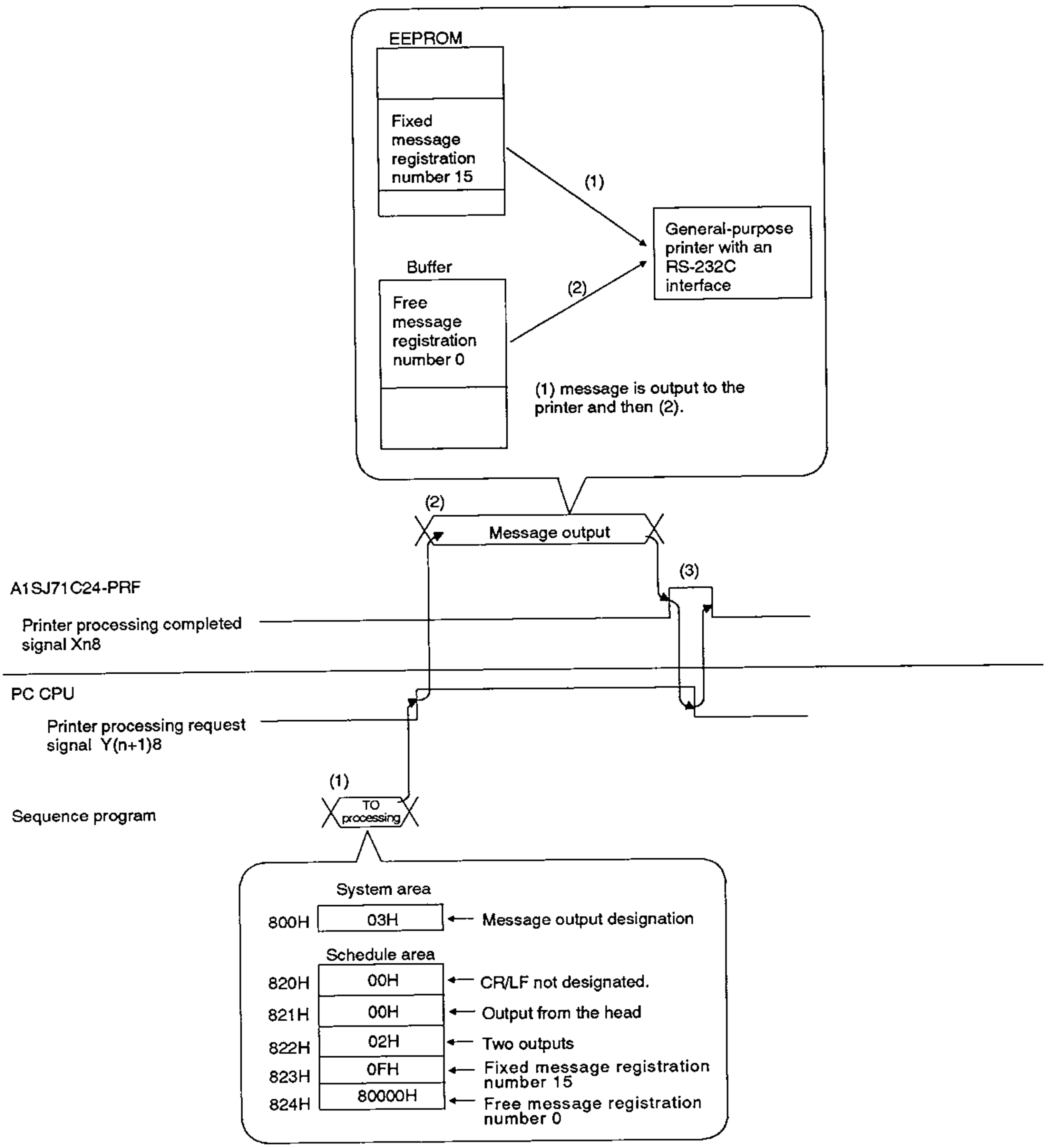


POINT

Section 11.5.2 gives details about schedule area item setting.

11.6.2 Message output timing

The following example explains the timing when registration number 15 of a fixed message and registration number 0 of a free message are output.



(1) Write a message output (03H) in buffer 800H with a sequence program, and set each item of a schedule area.

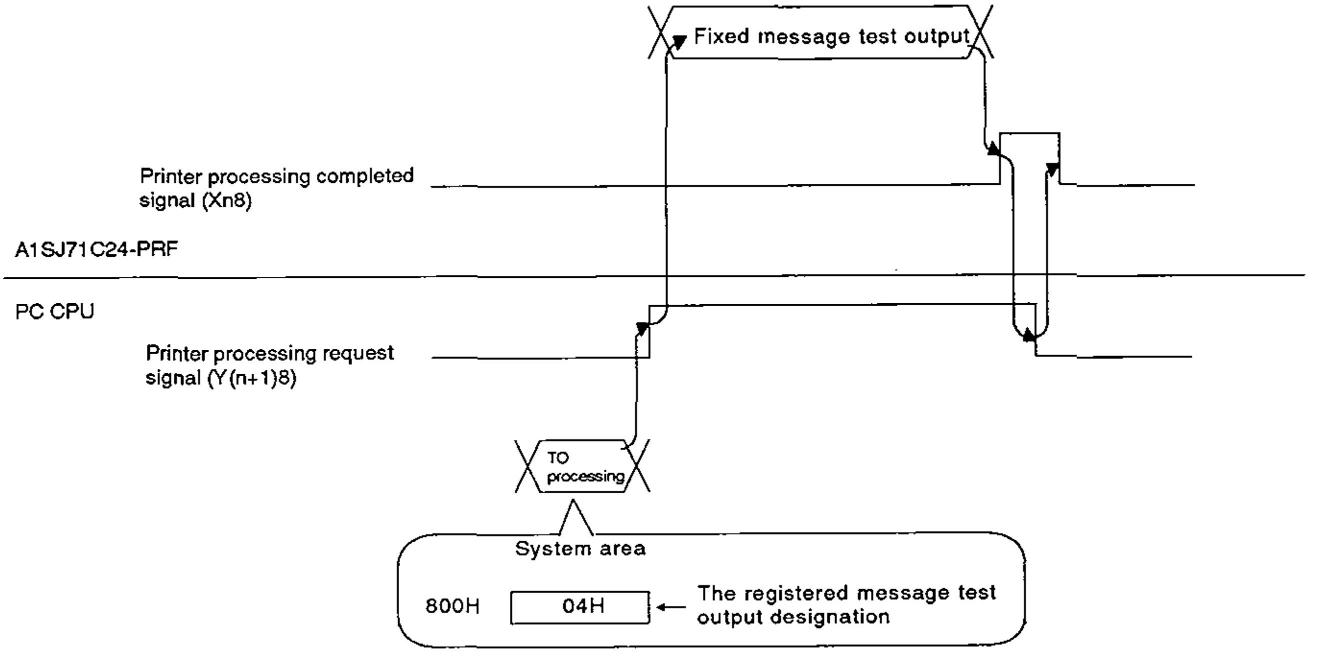
After writing to the buffer. use a sequence program to turn ON the printer processing request signal (Y(n+1)8).

(2) When the printer processing request signal (Y(n+1)8) goes ON, messages are output in the order set by the A1SJ71C24-PRF at the schedule area. After outputting is completed, the A1SJ71C24-PRF turns ON the printer processing completed signal (Xn8).

(3) After the printer function has turned ON the printer processing completed signal (Xn8), turn OFF the printer processing request signal (Y(n+1)8) with a sequence program.

11.7 Registered Message Test Output

A currently registered fixed message is output from registration number 1 to the printer by designating a registered message test output (04H) to buffer address 800H.



Registered message test output example

**** 001 ****

MITSUBISHI ELECTRIC

**** 002 ****

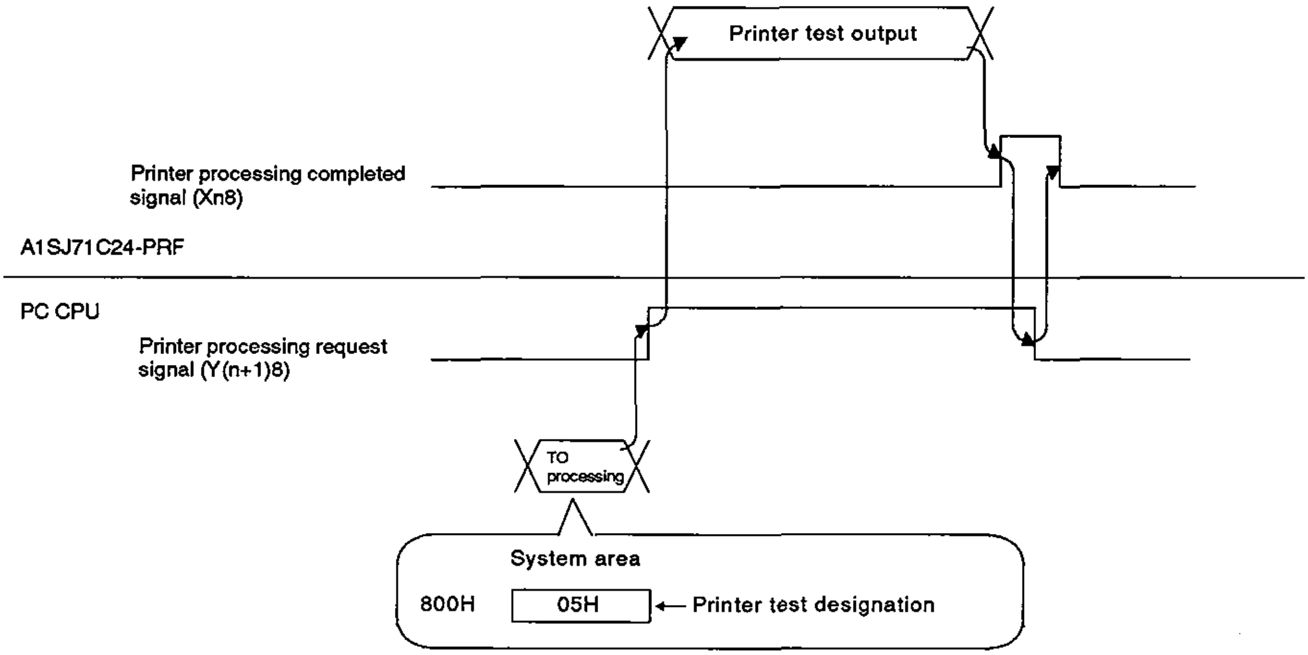
A1SJ71C24-PRF

**** 003 ****

PRINT SAMPLE

11.8 Printer Test

This function tests the printer output by designating a printer test (05H) to buffer address 800H.



Printer test example

!"#$%&'( )*+,-./0123456789:;<=>?@ABCDEFGHIJKLMNOPQRSTUVWXYZ[\ ]^ _'abcdefghijklmnopqrstuvwxyz{|} ¯

11.9 Example of a Printer Output Program Using the Printer Function

This section gives an example of a printer output sequence program using the printer function.

(1) Printer..........................General-purpose printer

(2) *Mode setting switch.....5*

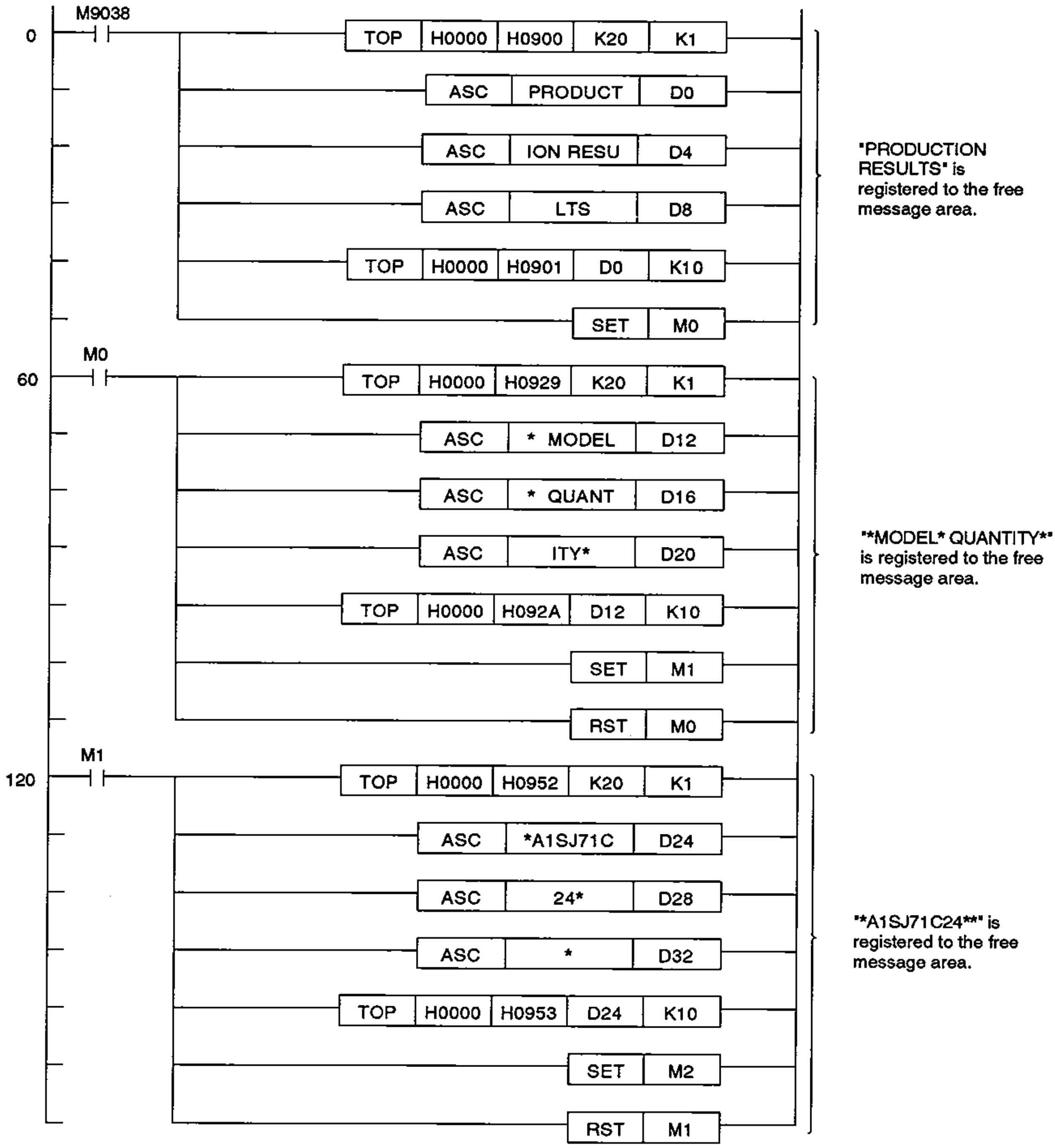
(3) Setting switch (for transmission specifications, etc.)

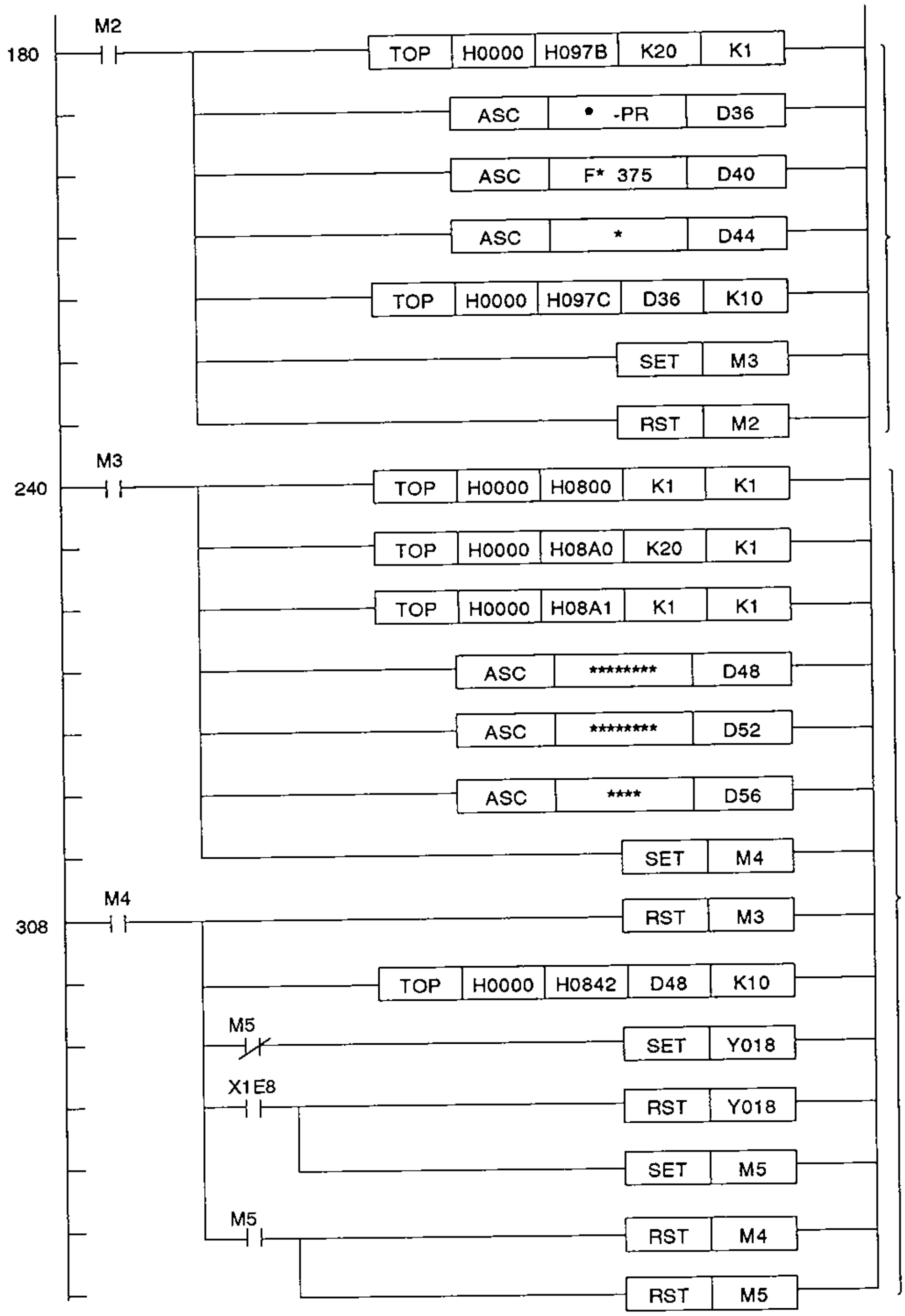
The manual of utilized printer gives details about settings, such as transmission specifications.

(4) *Output example*

```
  P R O D U C T I O N   R E S U L T S
* * * * * * * * * * * * * * * * * * * *
*     M O D E L     * Q U A N T I T Y *
* * * * * * * * * * * * * * * * * * * *
* A 1 S J 7 1 C 2 4 *                 *
*           - P R F *         3 7 5   *
* * * * * * * * * * * * * * * * * * * *
```

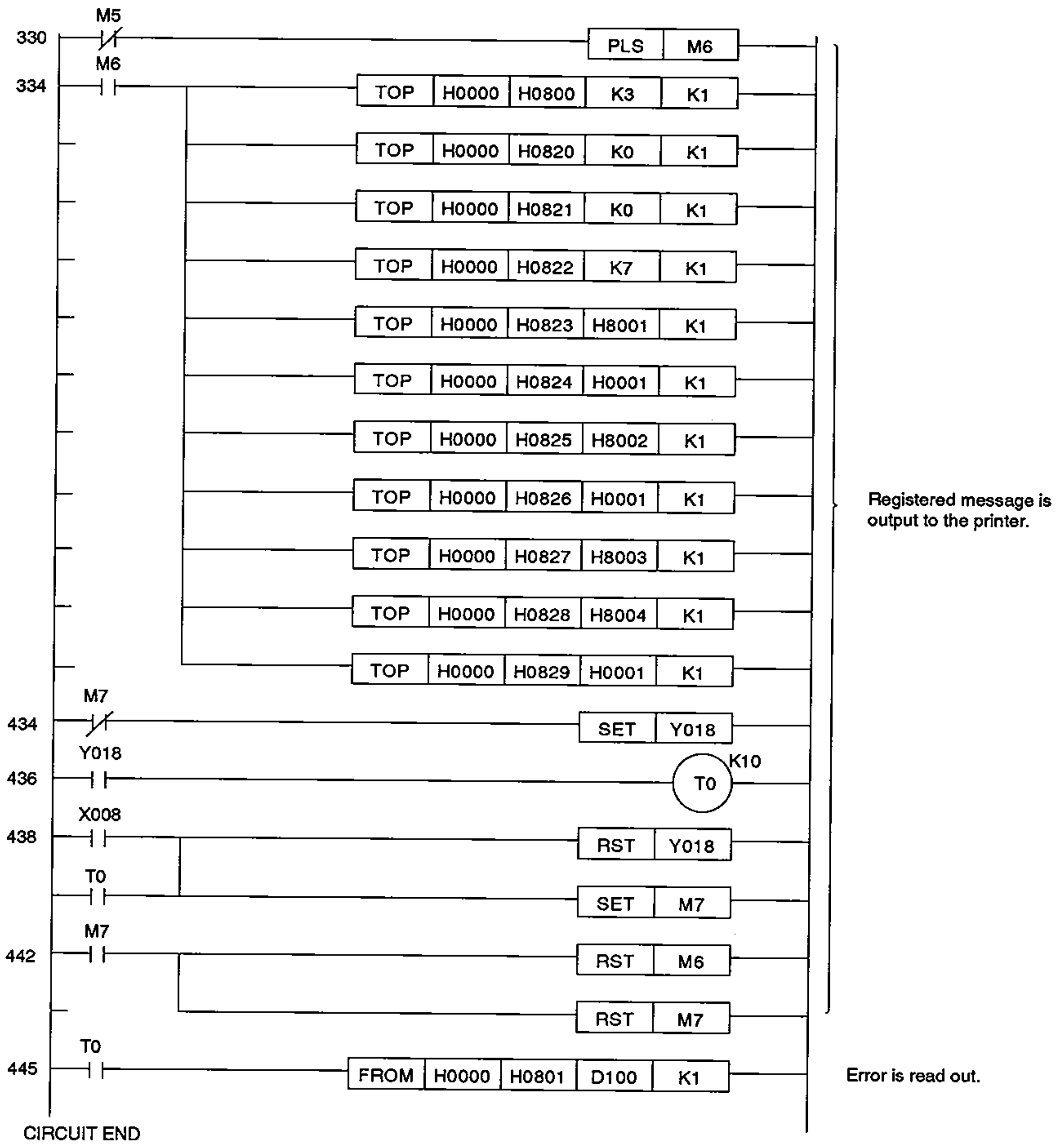
(5) Sequence program





"*-PRF* 375*" is registered to the free message area.

"********************" is registered to the fixed message area.


330 M5 PLS M6
334 M6 TOP H0000 H0800 K3 K1
TOP H0000 H0820 K0 K1
TOP H0000 H0821 K0 K1
TOP H0000 H0822 K7 K1
TOP H0000 H0823 H8001 K1
TOP H0000 H0824 H0001 K1
TOP H0000 H0825 H8002 K1
TOP H0000 H0826 H0001 K1
TOP H0000 H0827 H8003 K1
TOP H0000 H0828 H8004 K1
TOP H0000 H0829 H0001 K1
434 M7 SET Y018
436 Y018 T0 K10
438 X008 RST Y018
T0 SET M7
442 M7 RST M6
RST M7
445 T0 FROM H0000 H0801 D100 K1
CIRCUIT END
Registered message is output to the printer.
Error is read out.

[TROUBLESHOOTING]

This section describes the troubleshooting procedures for the CPU, computer link, and printer functions of the A1SJ71C24-R2 and A1SJ71C24-PRF.

12. TROUBLESHOOTING

This chapter describes errors which can occur with the A1SJ71C24 procedures.

12.1 NAK Error Codes with Dedicated Protocols

Table 12.1 gives the error codes and their descriptions when the NAK code is transmitted between the computer and the PC CPU as 2-digit ASCII (hexadecimal) between 00H and FFH.

If several errors occur simultaneously, the code with the lowest number takes precedence and is transmitted.

If any of the following errors occur, the transmission sequences are initialized and LED NEU (LED No. 8) is turned ON.

Table 12.1 Error Code List

Error Code (Hexadecimal)	Error	Error Description	Indicator LED No.	Corrective Actions
00H	Disable during RUN	Invalid access has been made during RUN. (1) Data has been written to a A1SCPU with the SW04 OFF (write disable during RUN). (2) Sequence program and parameters have been written.	C/N (LED No.11)	(1) Start communicationss after turning ON SW04. (2) Write parameters after setting the A1SCPU to STOP.
01H	Parity error	Parity error With the SW09 ON (parity enabled), the parity check result does not match the state of SW10 (odd/even parity).	P/S (LED No.12)	Check control protocol, change the SW setting or data.
02H	Sum check error	Sum check error With the SW12 ON (sum check enabled), the sum check result of received data does not match the sum check code of transmitted data, i.e., send data is different from received data.	P/S (LED No.12)	Check data transmitted from computer and sum check result. Correct invalid data.
03H	Protocol error	Communications protocol not valid. Communications have been made with a protocol different from the one set by the mode setting switch.	PRO (LED No.13)	Check and correct the mode setting switch position and control protocol and restart data communications.
04H	Framing error	Framing error Data does not match the setting of SW11 (stop bit).	SIO (LED No.14)	Change the setting of SW11 or the control protocol.
05H	Overrun error	Overrun error New data has been transmitted before A1SJ71C24 receives all the preceding data.	SIO (LED No.14)	Decrease the data transmission speed and restart data communications.
06H	Character area error	Character area A, B, or C error, or designated command does not exist. (1) The designation of the character area A, B, or C for the control protocol set with the mode setting switch is not correct. (2) A command used with the protocol does not exist. (For example, a subsequence program was designated to be used with A1SCPU.) The set device number does not exist in the set PC CPU. (3) The device number is not set with the required number of characters. (ACPU common command: 5 characters, AnACPU dedicated command: 7 characters)	PRO (LED No.13)	(1) Check and correct the character area A,B, or C and restart data communications. (2) See the functions list in Section 3.3.1 and the A1SCPU User's Manual to correct the designated commands, and restart data communications. (3) See Section 8.7.1 to correct the number of setti

Error Code (Hexadecimal)	Error	Error Description	Indicator LED No.	Corrective Actions
07H	Character error	Character error received. A character other than "A to Z", "0 to 9", "_" and control codes in Section 8.4.5 (1) has been	PRO (LED No.13)	Check and correct data.
08H	PC CPU access error	Buffer memory is unable to make communications with the PC CPU. The PC CPU is not the type mentioned in Section 2.2.	C/N (LED No.11)	Use a PC CPU which can perform data communications.
10H	PC CPU number error	Defined PC CPU number does not exist. The PC CPU number designated with the protocol was not the self (FFH) or a station number set with the MELSECNET link parameters.	C/N (LED No.11)	Change the PC CPU number to the self (FFH) or a station number set with the MELSECNET link parameters, and restart data communications.
11H	Mode error	Incorrect communications between an A1SJ71C24 and a A1SCPU. After the A1SJ71C24 has correctly received a request from the computer, normal data communications is not performed between the A1SJ71C24 and A1SCPU due to noise or some other reason.	—	Restart data communications. If the error recurs, (a) check for noise and/or other causes, or (b) replace the A1SJ71C24. Restart data communications.
12H	Special function module designation error	Special function module designation error. A special function module, having buffer memory and capable of performing data communications, is not placed in the designated special function module number's position. Or the module number is wrong.	C/N (LED No.11)	Check control protocol data or change the special function module location.
13H	Program step number designation error	Error in the designation of a sequence program step number. A step number was designated which lies outside the program range designated by the PC CPU parameters.	PRO (LED No.13)	Designate a step number which lies within the designated range, or change the parameters and restart transmission.
18H	Remote error	Remote RUN/STOP impossible. Remote STOP/PAUSE has already been executed from another module (such as another A1SJ71C24).	PRO (LED No.13)	Check for and reset remote STOP/PAUSE from another module.
20H	Data link error	Access was made to a station with which communications has been discontinued.	C/N (LED No.11)	Check the state of data link.
21H	Special function module bus error	Memory access to the special function module cannot be made (for command TR, TW). (1) Special function module control bus error. (2) Special function module breakdown.	C/N (LED No.11)	A1SCPU, base unit, special function module or A1SJ71C24 hardware fault. Consult the nearest Mitsubishi representative.

REMARKS

(1) Error codes 00H to 08H are transmitted to a computer after diagnosis by an A1SJ71C24, when access is made by the computer to the A1SJ71C24.

(2) Error codes 10H to 21H are transmitted from an A1SJ71C24 to a computer after diagnosis by a PC CPU when access is made by an A1SJ71C24 to the PC CPU.

12.2 Bidirectional Mode Error Codes

Table 12.2 gives the error codes, error descriptions, and corrective actions for errors which may occur during bidirectional mode communications.

The following error codes (1-word integers) are transmitted in order of the lower byte and the higher byte immediately following the NAK code when an error has occurred. (e.g., when the error code is 01_H, 01_H is transmitted first, and then 00_H is transmitted.)

Table 12.2 Error Code List

Error Code (Hexadecimal)	Error Descriptions	Corrective Actions
01H	Send data length error	Either (a) make the setting size of the send data length storage area in the buffer memory for bidirectional transmission smaller than the size of the send data storage area, or (b) set the send data length to "1" or greater. (Data which does not have a data part cannot be transmitted using the bidirectional mode.)
02H	Response message time-out error	Set the computer so that it transmits the response message (in response to the data received from the A1SJ71C24) to the A1SJ71C24 within the set value of the time-out time setting area (address 113H) in the A1SJ71C24 buffer memory.
03H	Simultaneous transmission error	Either (a) interlock the computer with the A1SJ71C24 so that they cannot begin transmitting data simultaneously to each other, or (b) set the data valid/invalid setting area (address 114H) in the A1SJ71C24 buffer memory to "valid".
10H	Error code is not received when the NAK code is received	When the computer transmits the NAK code to the A1SJ71C24 in response to the data received from the A1SJ71C24, an error code should be added immediately after the NAK code.
22H~5FH	Errors designated by the user	These error codes are added to immediately after the NAK code. Take corrective actions according to the procedure fixed by user.
80H	SIO error at data receive Framing error Overrun error	• Transmit data from the computer according to the following settings with the A1SJ71C24 (see Section 4.3.2 for SW04 to SW11). • Data bit length with SW08 • Transmission speed with SW05 to SW07 • Stop bit length with SW11 • Use insulation transformers (noise-cutting transformers) to eliminate noise.
81H	Check sum error Parity error (only at data receive)	• To transmit the check sum to the A1SJ71C24, obtain the check sum as described in Section 10.5.2. Set the check sum enable/disable setting area (address 115H) in the A1SJ71C24 buffer memory to "disable", so that the check sum is not transmitted. • Transmit data from the computer according to settings with SW09 and SW10 of the A1SJ71C24.
83H	Received data length error	Either (a) make the data part length and the set value of the data part length of the receive message less than the size of the received data storage area, or (b) transmit correctly the data length (0001H or more) contained in the message which is transmitted to the A1SJ71C24. (Data which does not have the data part cannot be transmitted using the bidirectional mode.)
83H	Received data time-out error	When data is transmitted from the computer, set the actual length of the data part to the data length part. (The A1SJ71C24 executes the time-out check (as set with address 113H of the buffer memory) if it fails to receive data of a set length. This error occurs when it fails to receive the next data within the set time.)

12.3 Error codes when using a printer function

Table 12.3 gives the error codes, error contents, and corrective actions for errors which occur when using a printer function.

Processing is not executed if any of these errors occur.

To restart process execution, write 00H to buffer address 801H. (This must be done when a printer processing request signal (Y1F8) is OFF.)

Table 12.3 Error Code List

Error Code (Hexadecimal)	Error Descriptions	Corrective Actions
00H	No error	—
01H	Function designation error	The function designation made from the computer or PC CPU is different from that designated at buffer address 800H. Designate the correct function from the computer or PC CPU.
02H	Designated number error	The designated message number is not in the following range: 0 < Designated number ≤ 400 Set the designated number in this range.
03H	Number of characters error	The designated number of characters is not in the following range: 0 < Number of characters ≤ 80 Set the number of characters in this range.
04H	Number of outputs error	The designated number of outputs is not in the following range: 0 < Number of outputs ≤ 99 Set the number of outputs in this range.
05H	Message designation error	The designated message does not exist in the free/fixed message areas. Designate a correct message.
06H	EEPROM error	The message registered in the EEPROM is different from the one before registration.
07H	Interruption	Y(n+1)C goes ON, and the printer output is interrupted. Turn Y(n+1)8 OFF to restart the printer.
08H	Printer processing error	After the printer processing request signal (Y(n+1)8) was turned ON, the printer processing completed signal (Xn8) was turned ON before the printer processing request signal (Y(n+1)8) was turned OFF.
09H	Mode setting error	The mode setting switch is not set to a number from "5" to "8". Set it to "5" to "8".
FFH	Buffer write error	An error occurred during data communications with a PC CPU. Reset the A2CCPUC24 (-PRF) and retry communications.

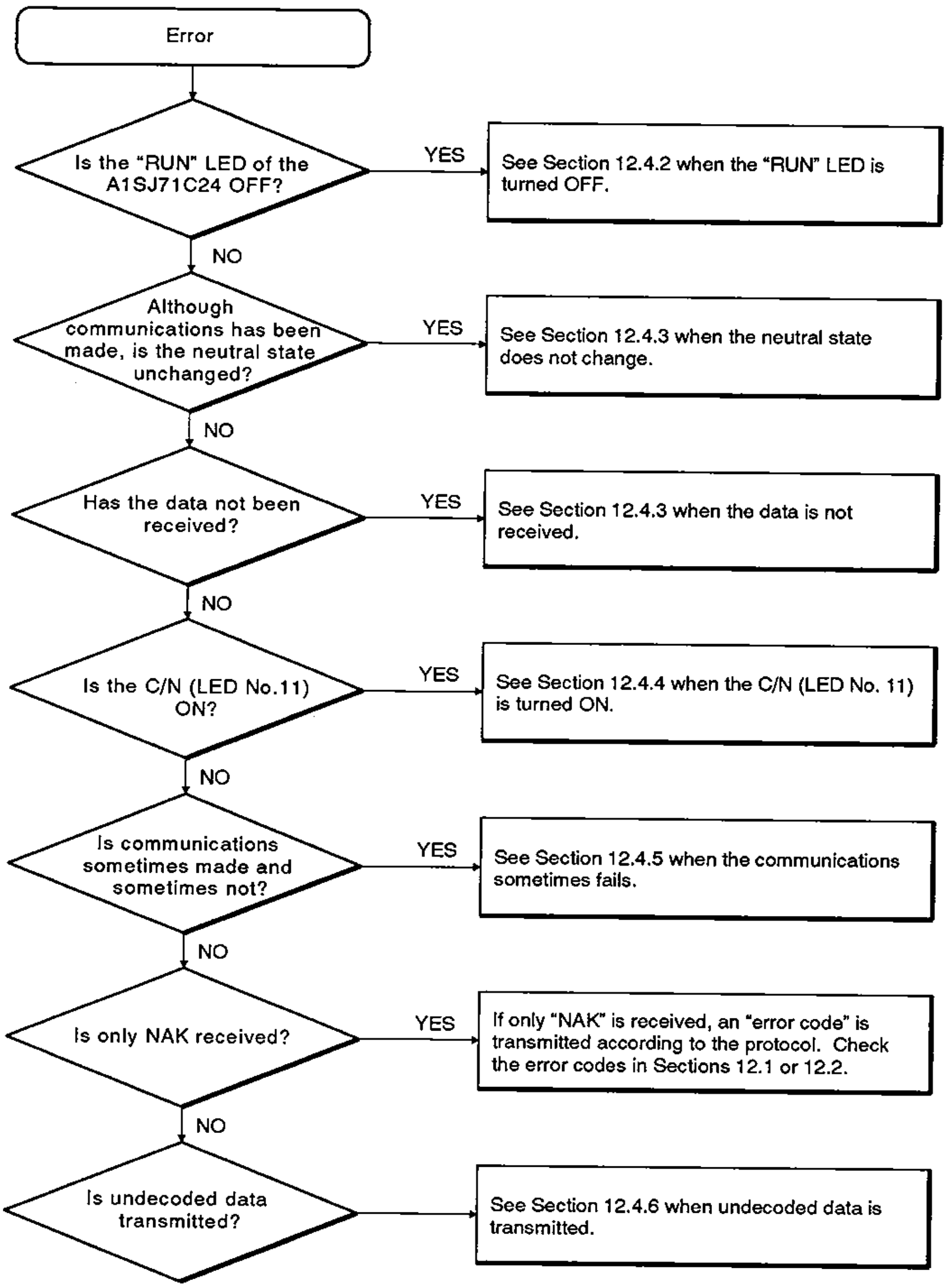
12.4 Troubleshooting OFF

This section describes basic troubleshooting procedures for the A1SJ71C24. The User's Manuals give information on PC CPU module troubleshooting.

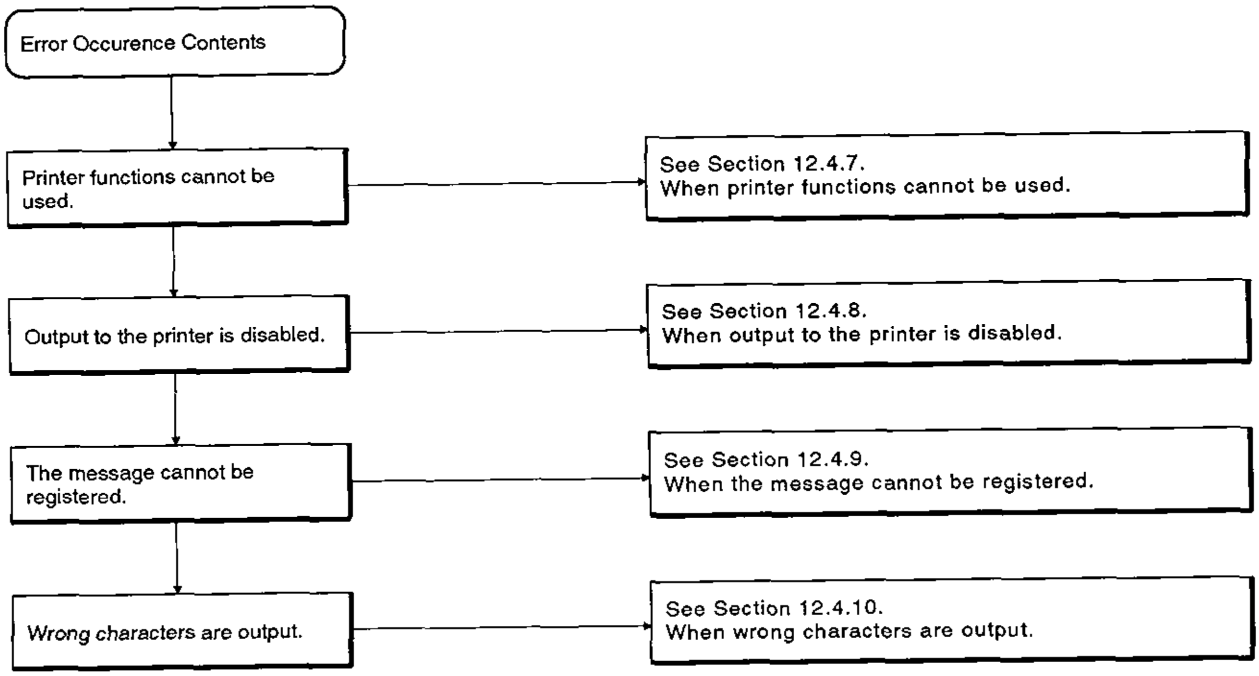
12.4.1 Troubleshooting flow chart

The state of errors is described as follows:

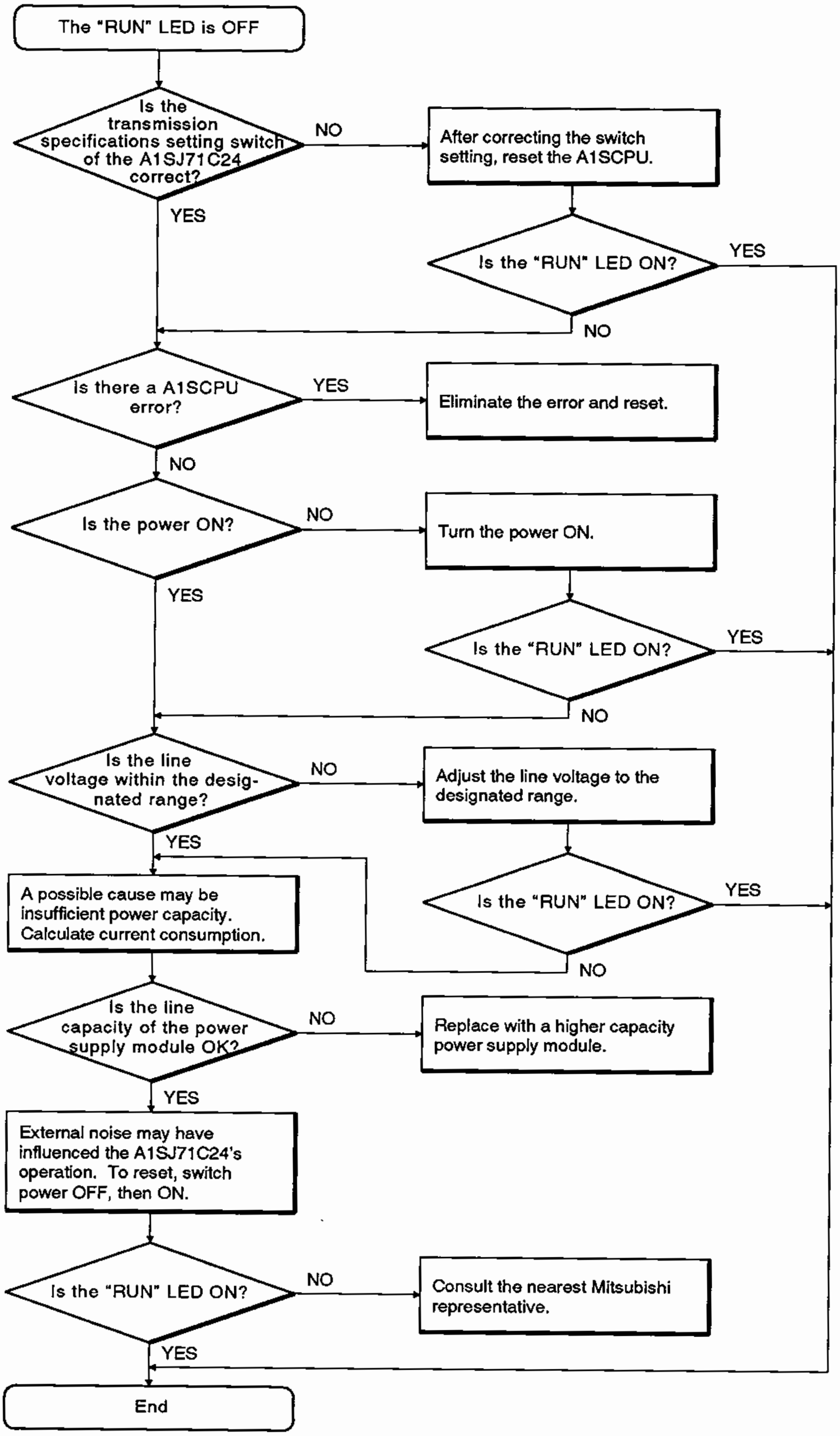
(1) Computer link function



(2) Printer functions

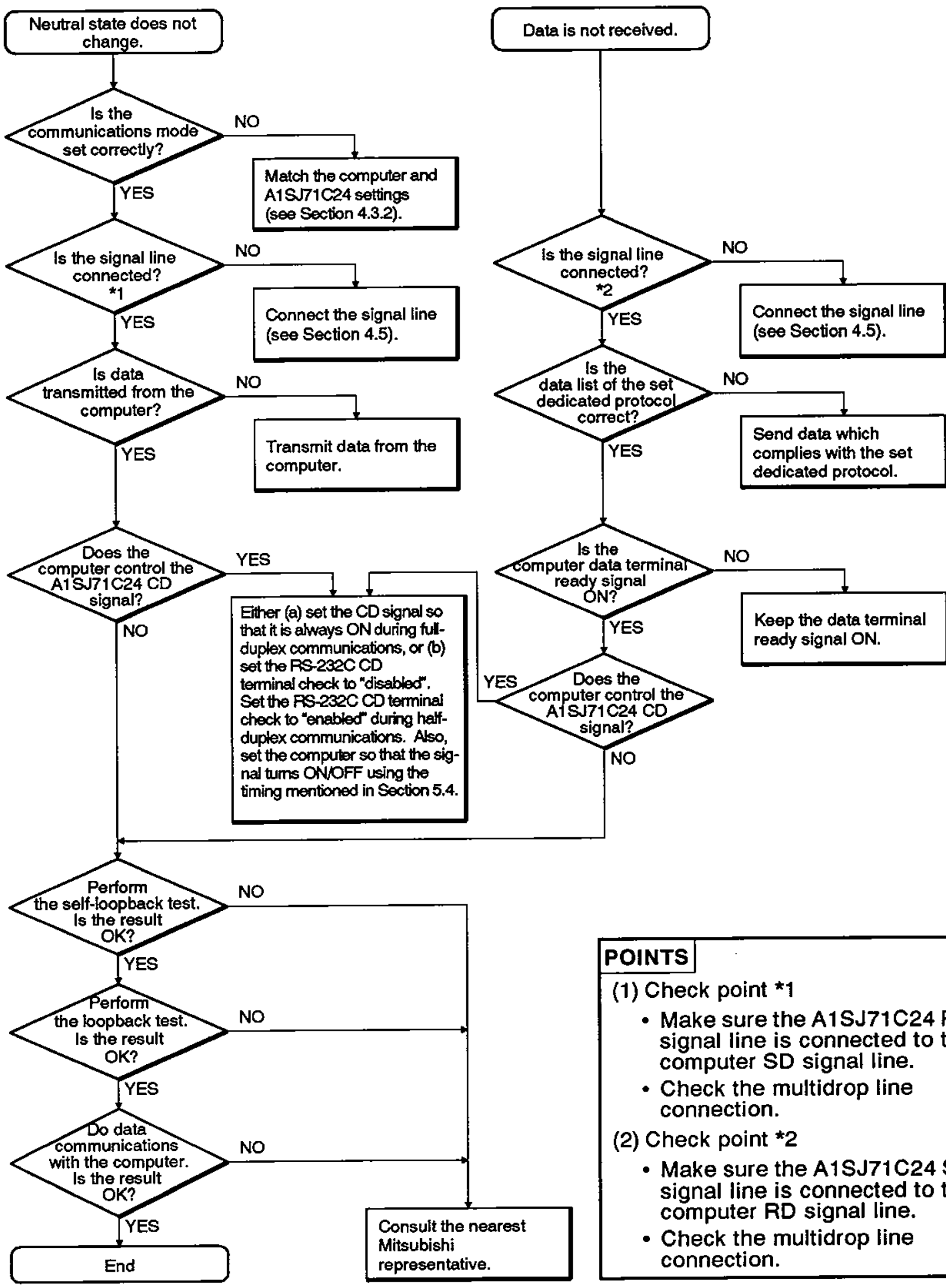


12.4.2 When the "RUN" LED is turned OFF



12.4.3 When the neutral state does not change or data is not received

The A1SJ71C24 LED remains ON indicating (a) the neutral state, or (b) that communications is disabled (even though a communications request is made to the A1SJ71C24). The computer cannot receive data.



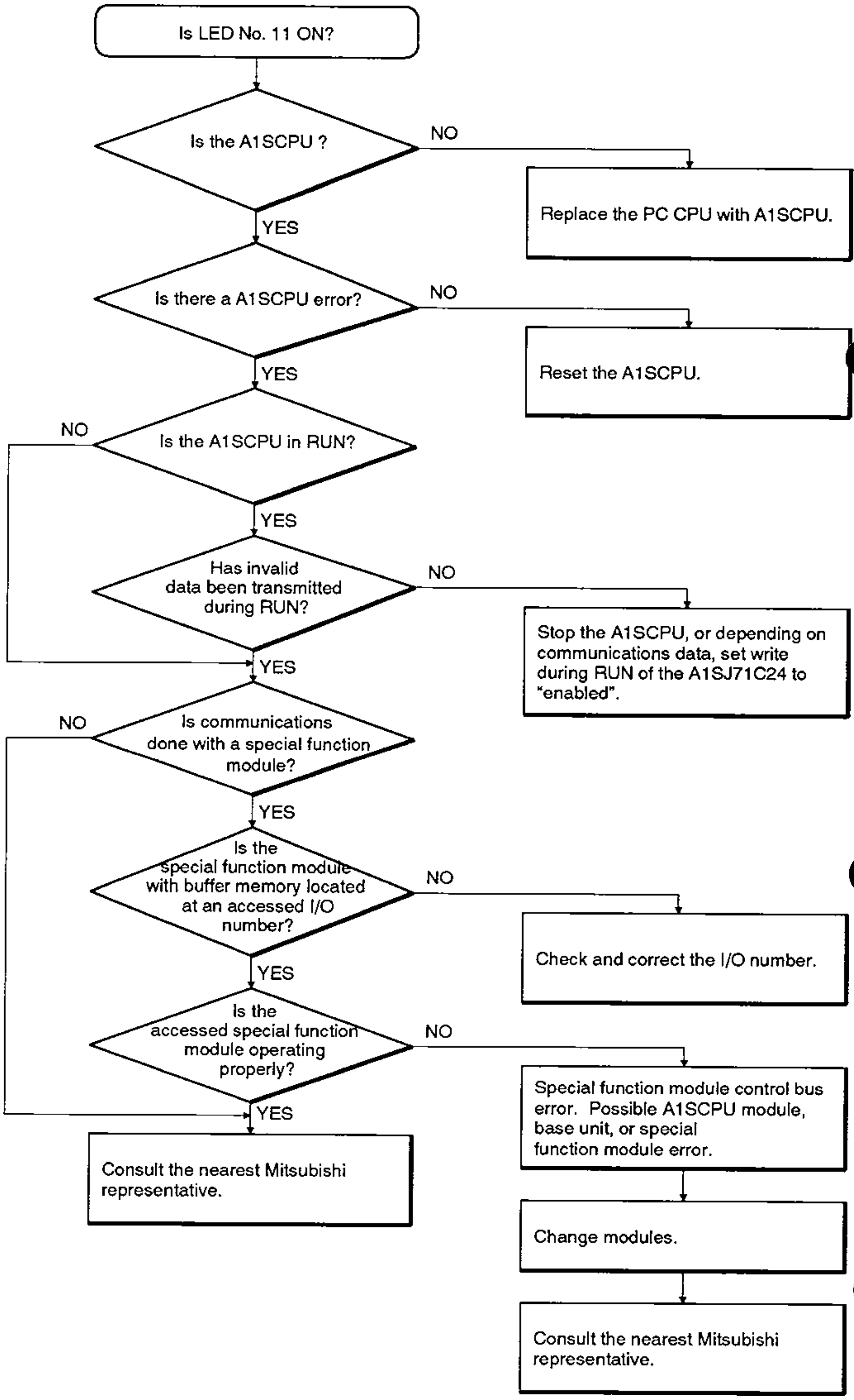
POINTS

(1) Check point *1
- Make sure the A1SJ71C24 RD signal line is connected to the computer SD signal line.
- Check the multidrop line connection.

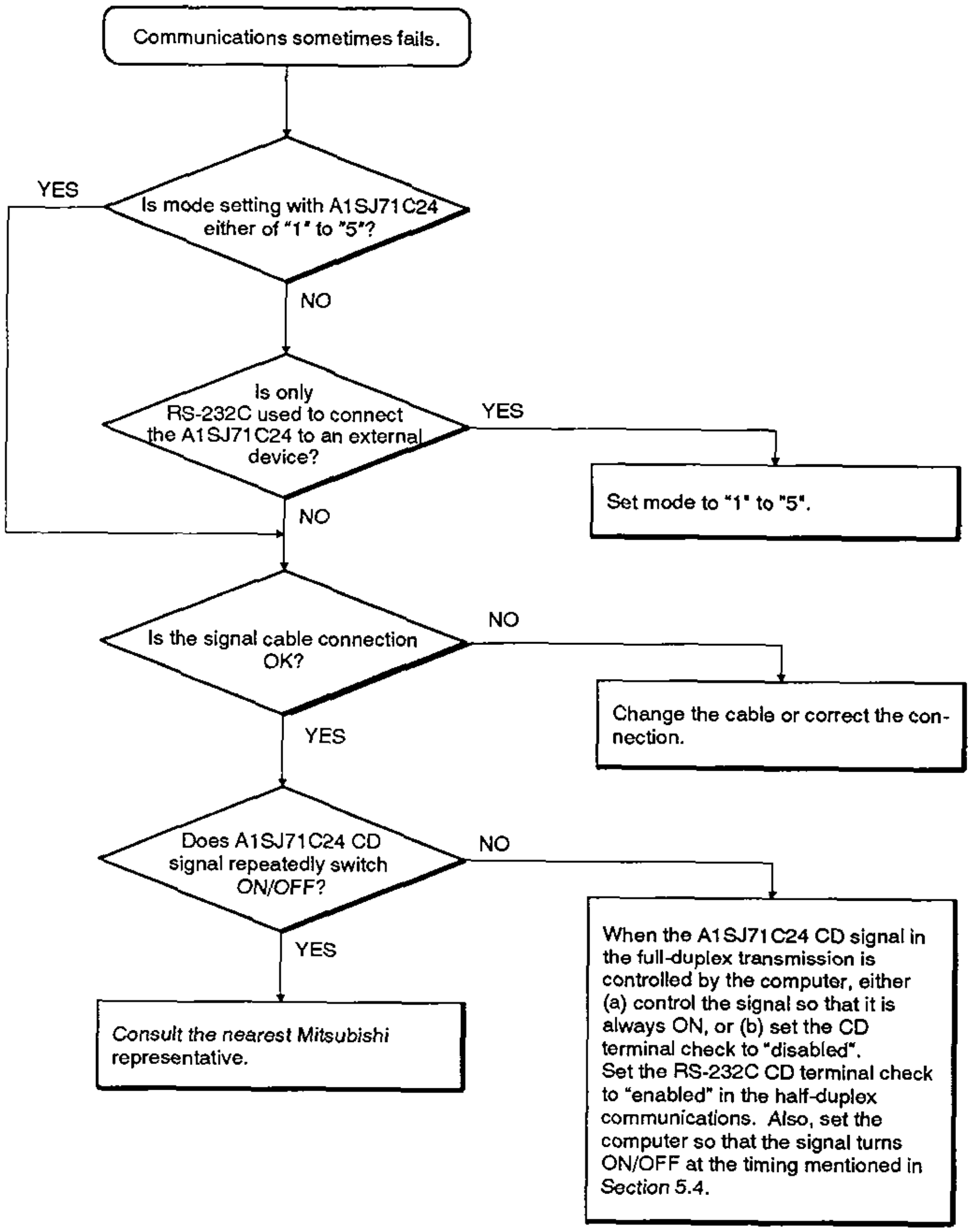
(2) Check point *2
- Make sure the A1SJ71C24 SD signal line is connected to the computer RD signal line.
- Check the multidrop line connection.

12.4.4 When the C/N (LED No. 11) is turned ON

Flow chart to use when the C/N (LED No. 11) on the A1SJ71C24 panel turns ON.

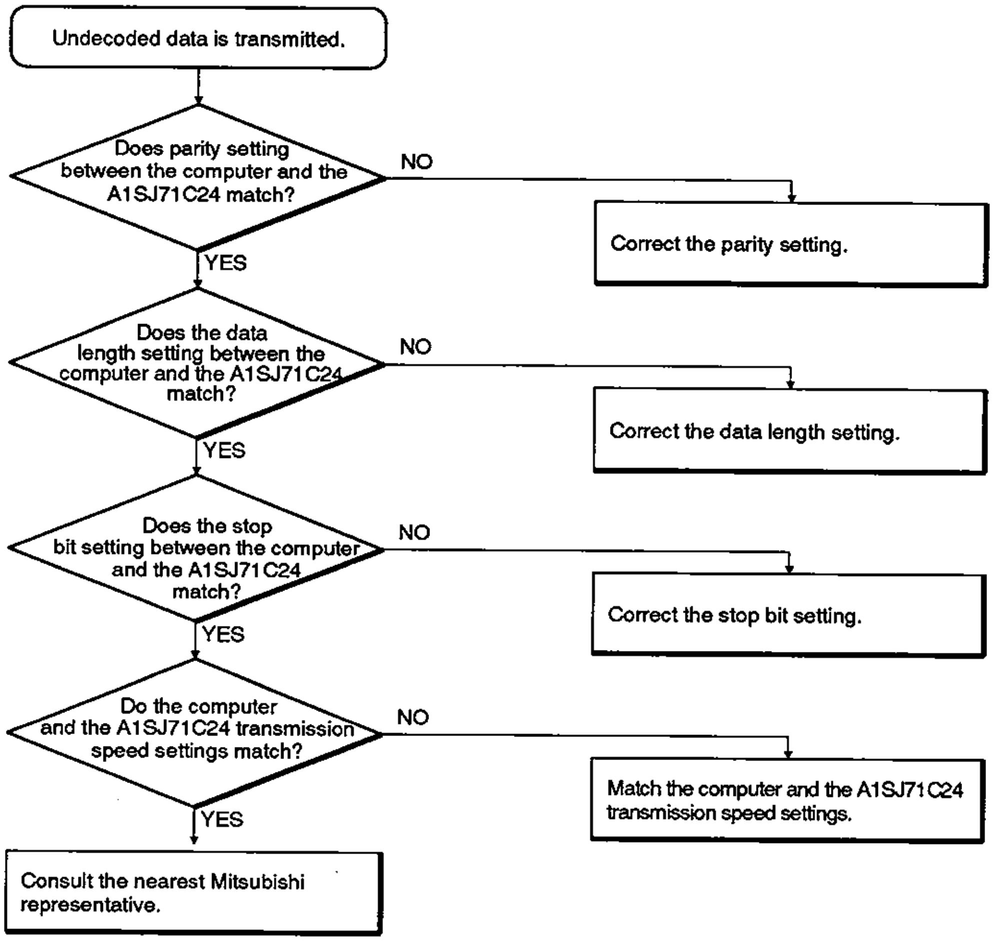


12.4.5 When communications sometimes fails

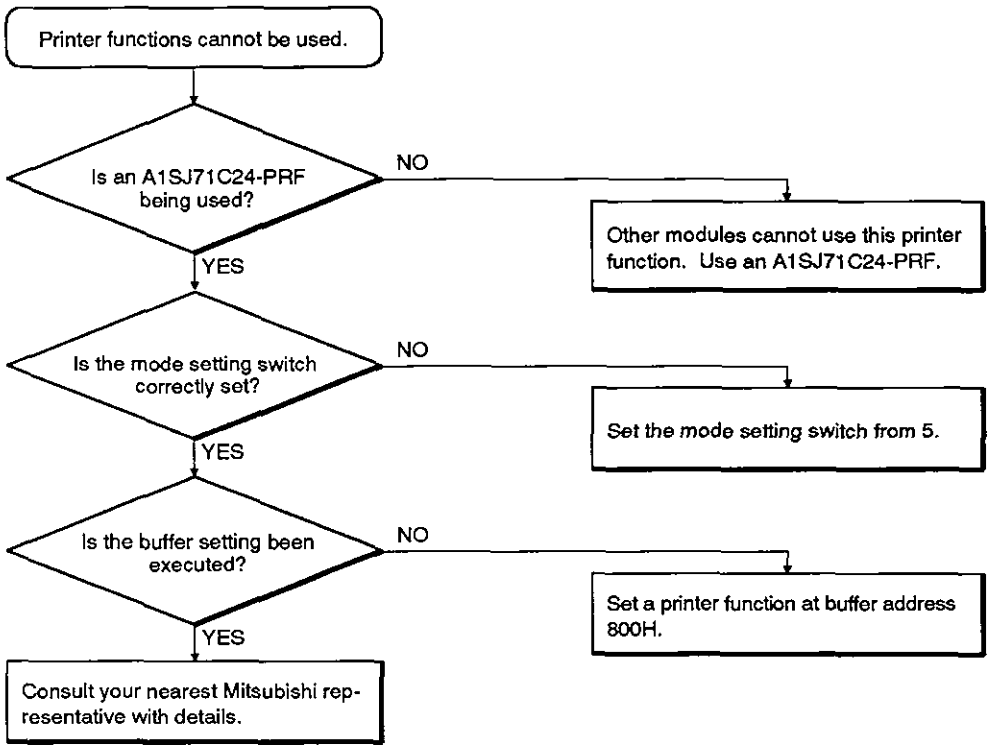


12.4.6 When undecoded data is transmitted

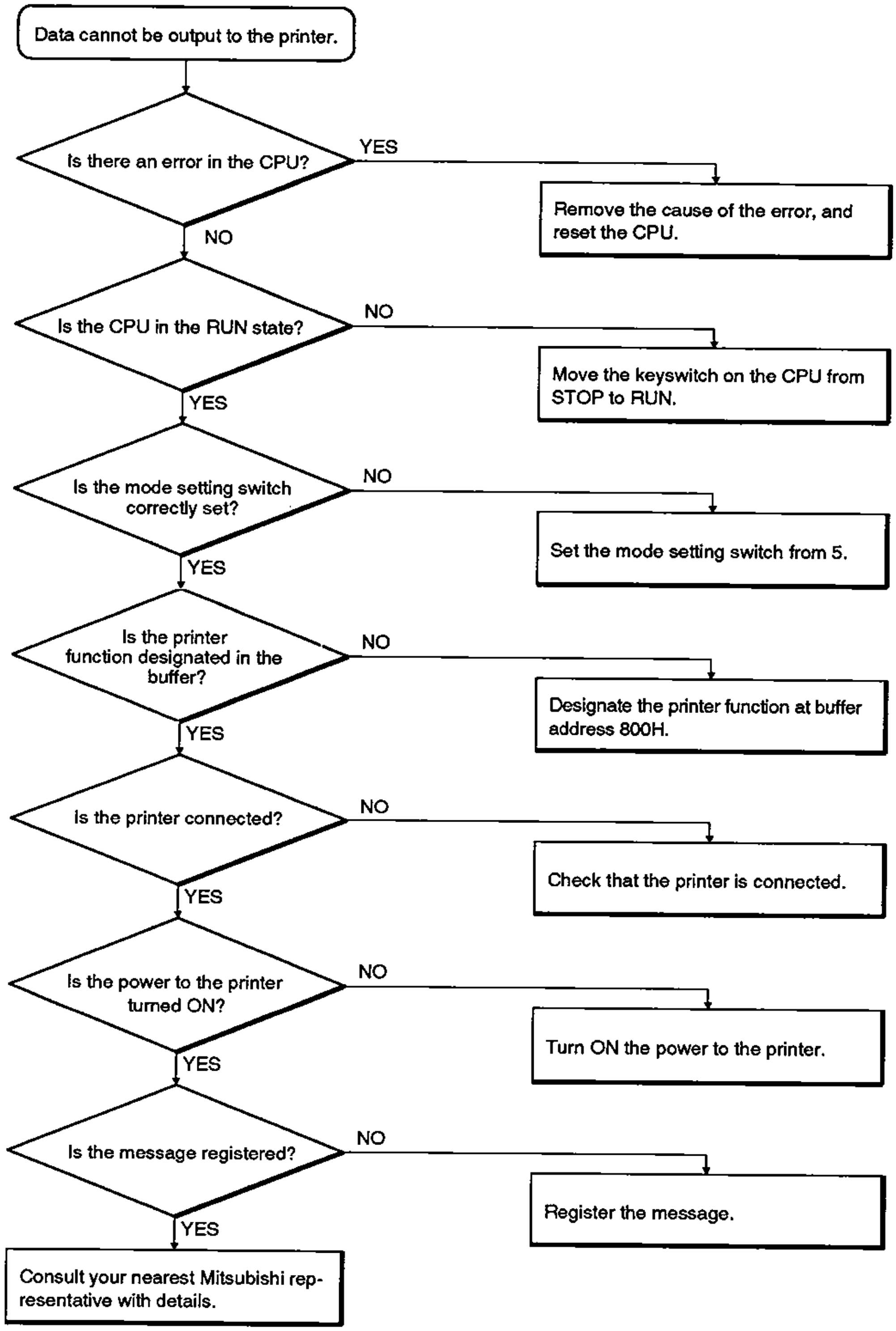
Use this flow chart when the A1SJ71C24 (in response to data from the computer) transmits code and data which is not included in the control code.



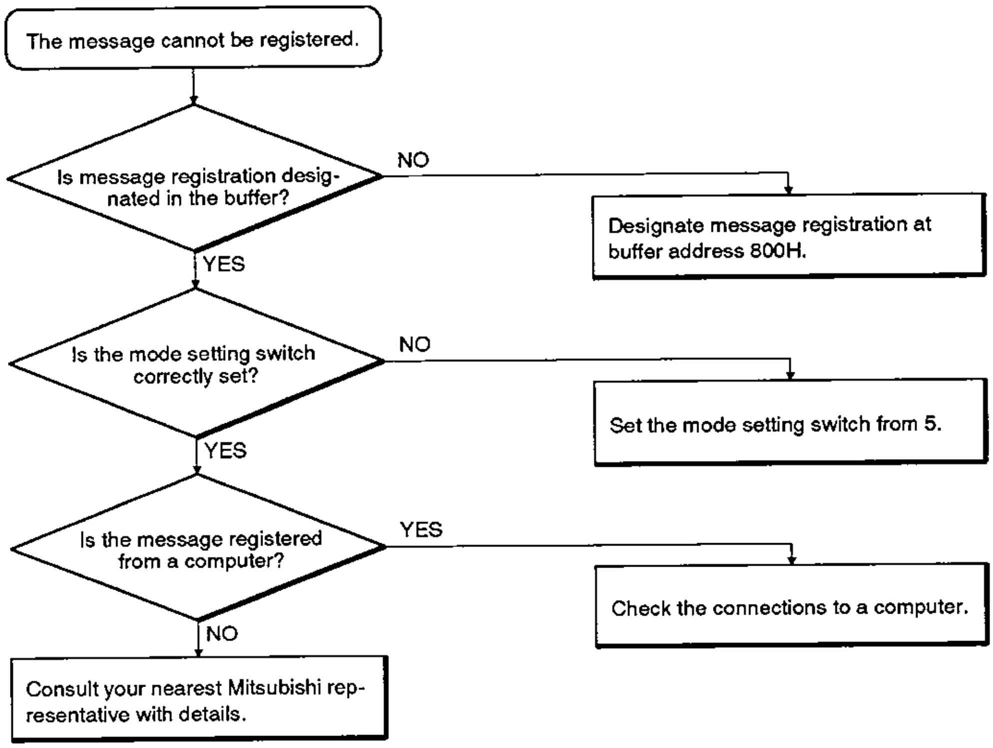
12.4.7 When printer functions cannot be used



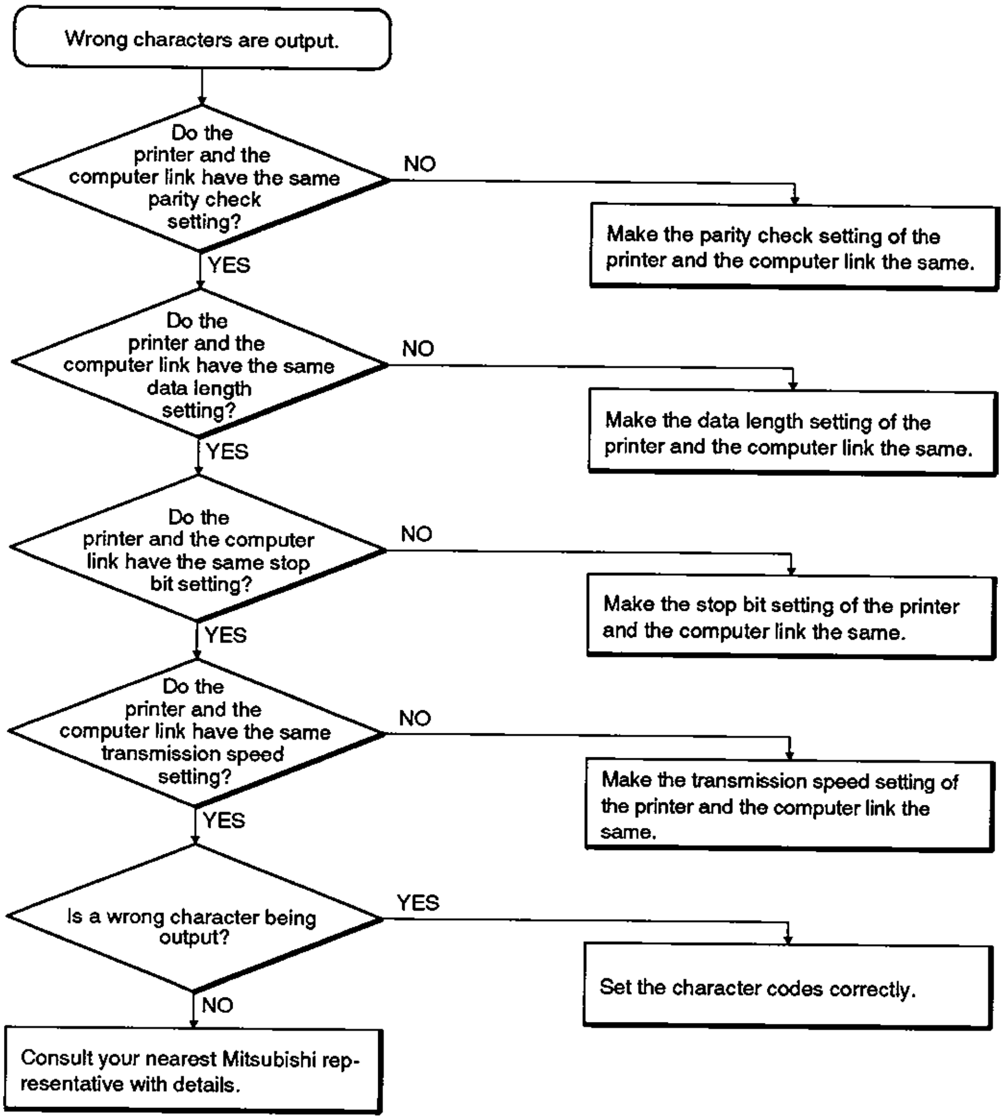
12.4.8 When output to the printer is disabled



12.4.9 When the message cannot be registered



12.4.10 When wrong characters are output



[APPENDICES]

This section explains compatibility with an A1SJ71C24-S6, communications time between a CPU and a computer link, and the A-series special-function module buffer addresses.

APPENDICES

APPENDIX 1 PRECAUTIONS CONCERNING COMPATIBILITY AND THE USE OF EXISTING PROGRAMS PREPARED FOR THE AJ71C24-S6 COMPUTER LINK MODULE

The following sections describe precautions which should be taken when using the A1SJ71C24-R2 computer link module or the A1SJ71C24-PRF computer link/printer function module (hereafter called the A1SJ71C24).

These precautions cover compatibility with the AJ71C24-S6 computer link module (hereafter called the AJ71C24-S6), the use of existing programs prepared for the AJ71C24-S6, and procedures for changing, adding, and installing modules to the existing network.

1.1 Compatibility

The A1SJ71C24 and the AJ71C24-S6 use the same basic programs (PC CPU programs and computer programs).

However, m:n data communications cannot be done using an RS-422.

(The A1SJ71C24 has no RS-422.)

1.2 Precautions When Using Existing Programs

The following describes the precautions to take when the A1SJ71C24 is replaced by the AJ71C24-S6.

(1) The time required for communications with a PC CPU differs between the A1SJ71C24 and the AJ71C24-S6. The User's Manual for each type of module gives details.

(2) Since the A1SJ71C24 has no RS-422, m:n data communications cannot be done using an RS-422.

1.3 Function Comparison

The following table gives the function comparison between the A1SJ71C24 and the AJ71C24-S6:

Function \ Module	AJ71C24-S6	A1SJ71C24	See Section
Mode switching	–	When the PC CPU is on line, the dedicated protocol format is selected from 1 to 4 and the mode is switched between the no-protocol and the bidirectional modes.	6 7.6
DC code control		Controls the transmission/receive using the DC1 to DC4.	7.7 APP 6

APPENDIX 2 ASCII CODE TABLE

Character codes used for the computer link are shown below. (7-bit codes)

LSD \ MSD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	NUL	DLE	SP	0	@	P	`	p
1	0001	SOH	DC1	!	1	A	Q	a	q
2	0010	STX	DC2	"	2	B	R	b	r
3	0011	ETX	DC3	#	3	C	S	c	s
4	0100	EOT	DC4	$	4	D	T	d	t
5	0101	ENQ	NAK	%	5	E	U	e	u
6	0110	ACK	SYN	&	6	F	V	f	v
7	0111	BEL	ETB	/	7	G	W	g	w
8	1000	BS	CAN	(	8	H	X	h	x
9	1001	HT	EM	)	9	I	Y	i	y
A	1010	LF	SUB	*	:	J	Z	j	z
B	1011	VT	ESC	+	;	K	[	k	{
C	1100	FF	FS	,	<	L	\	l	|
D	1101	CR	GS	–	=	M	]	m	}
E	1110	SO	RS	.	>	N	↑	n	~
F	1111	SI	VS	/	?	O	←	o	DEL

APPENDIX 3 DTR CONTROL

This appendix explains DTR control.

(1) Explanation of DTR control

DTR control enables and disables data communications with an external device via the A1SJ71C24 RS-232C by means of the DSR and DTR signals.

(2) Data received from an external device is stored in the A1SJ71C24 no-protocol receive buffer memory area via the OS memory area.

Under the following conditions, the A1SJ71C24 temporarily stores received data to its OS area. When transfer to the no-protocol receive buffer memory is enabled (read request signal Xn1 is OFF), data is transferred until the receive completed code is received, or until the fixed length of data has been transmitted.

Conditions:

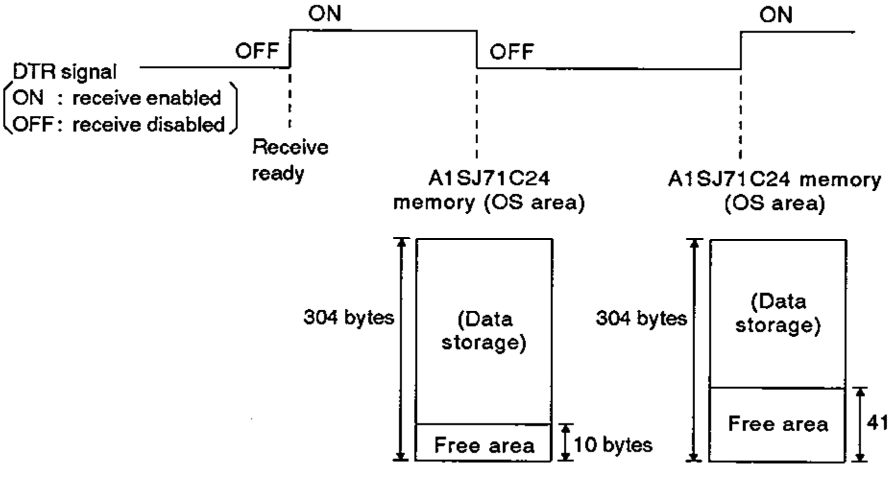
1) When there is too much data for the buffer memory because the received data length exceeds the no-protocol receive buffer memory area.

2) When data is transmitted from an external device before the PC CPU reads the data received previously.

(3) The size of the receive data storage area of A1SJ71C24 OS area is 279 bytes. It turns the DTR signal ON and OFF as follows:

- less than 10 bytes storage area free : OFF
- more than 41 bytes storage area free : ON

(4) When received data is cleared as described in Section 9.5 (5), all data in the OS area is cleared at the same time as data in the no-protocol receive buffer memory area.



APPENDIX 4 DC CODE CONTROL

This section explains DC code control done by the OS of an A1SJ71C24 when the DC code control is specified in the send control specification area (buffer address 11AH) of an A1SJ71C24. This control operation can be executed at data receive in the no-protocol/bidirectional mode using the RS-232C of the A1SJ71C24.

The figures in this section assume a no-protocol mode.

A control code (ENQ, ACK, NAK, check sum, and error code) is included in the bidirectional mode data.

4.1 DC1/DC3 Send Control

(1) DC1/DC3 is used to inform an external device whether DC1 and DC3 have been received.

(2) The control data is the same as the DTR control shown in Appendix 5.

An A1SJ71C24 transmits DC1 or DC3 to the external device instead of turning the DTR signal ON and OFF.

The DTR control of Appendix 5 gives details about send timing of DC1 and DC3.

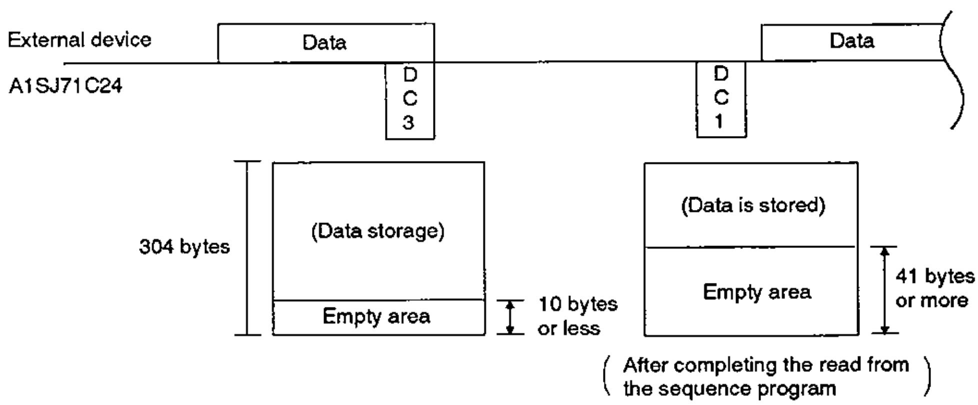
The DTR signal ON or OFF signals are expressed as follows in this manual.

(The DTR control)		(DC1/DC3 control)
DTR signal OFF	=	DC3 transmission
DTR signal ON	=	DC1 transmission

(3) DC1/DC3 send control can only be done using full-duplex communications.

(4) Do not include DC1/DC3 in the send data specified by the user.

(5) When an OS receive area cannot store received data, until storage of that received data is enabled, that received data is ignored.



POINTS

(1) When the power supply is turned ON or the PC CPU is reset, DC1 is not transmitted to the external device.

The state is the same as when DC1 was transmitted.

(2) If transmitted, DC1/DC3 can be switched.

Section *.* gives switching method details.

4.2 DC2/DC4 Send Control

(1) DC2/DC4 send control is discussed below.

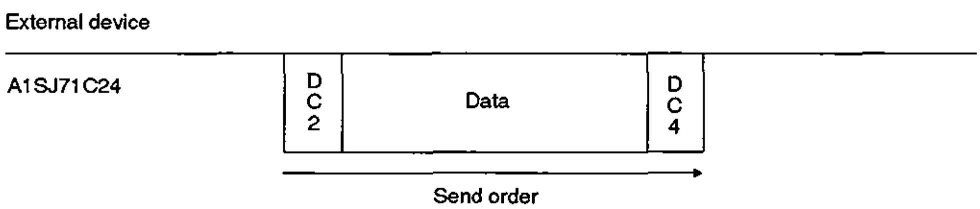
The A1SJ71C24 adds DC2 to the head of the transmitted data and DC4 to the end of the transmitted data under the following two conditions:

(a) When data is transmitted from the A1SJ71C24 to an external device.

(b) When response data (ACK/NAK) is transmitted for data receive in a bidirectional mode

(2) DC2 and DC4 are not included in the data the user transmits from an external device to the A1SJ71C24.

If it is necessary to include DC2 and DC4 in data, do not do receive control of DC2/DC4.



4.3 DC1/DC3 Receive Control

(1) DC1/DC3 receive control is send control under the following circumstances:

When data is transmitted from the A1SJ71C24 to an external device and when response data (ACK/NAK) is transmitted for data receive in the bidirectional mode

(a) When DC3 is received from the external device, the A1SJ71C24 interrupts the data send.

The user cannot access the received DC3.

(b) When DC1 is received from the external device, the A1SJ71C24 restarts the data send.

Transmitted data that was interrupted by receiving DC3 is transmitted.

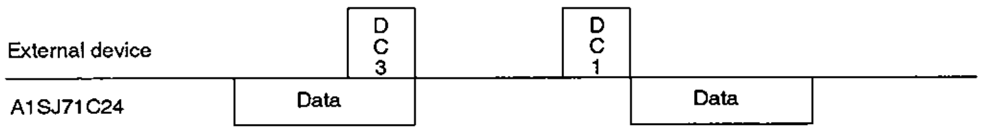
The user cannot access the received DC1.

(2) When DC1 is received, until the following DC3 is received, received DC1 is processed as data.

(3) When DC3 is received, until the following DC1 is received, received DC3 is processed as data.

(4) When received data cannot be stored in an OS receive area, that received data is ignored until the following received data is stored.

(5) DC1/DC3 receive control can only be done using full-duplex communications.



POINT

When the power supply is turned ON or the PC CPU is reset, DC1 is not received form the external device.

The state is the same as when DC1 was received.

4.4 DC2/DC4 Receive Control

(1) DC2/DC4 receive control is discussed below.

When an A1SJ71C24 receives data from the external device, the A1SJ71C24 stores the following data in an A1SJ71C24 buffer or a receive area for OS as valid data.

The data is data supplemented by DC2 and DC4.

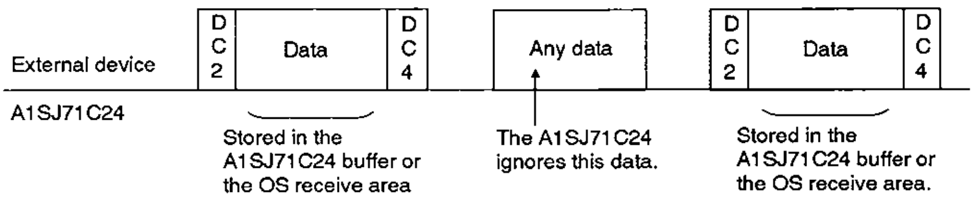
In this case, the user cannot access the received DC2/DC4.

(2) When DC2 is received, until DC4 is received, received DC2 is processed as data.

(3) When DC4 is received, until DC2 is received, all received data is disregarded as invalid data.

(4) DC2 and DC4 cannot be included in user data which is transmitted from an external device to the A1SJ71C24.

When it is necessary to include DC2 and DC4, do not do receive control of DC2/DC4.



APPENDIX 5 COMMUNICATIONS TIME BETWEEN AN A1SCPU AND AN A1SJ71C24

When the A1SCPU is in the run state, data is processed after executing the END instruction in response to a request from the A1SJ71C24. Section 3.3.1 gives the minimum number of devices processed per communications.

The intervening times (i.e. by how much the scan time increases) for each processing operation and its corresponding processing times (indicated in number of scans) are shown below.

Item				Command	Intervening Times (Scan Time Increases)		Scan Count Required for Processing
					A1S	Access Data Unit	
Device data	Device memory	Batch read	Bit units	BR	0.76 ms	256 devices	1 scan (2 scans for device "R" only)
			Word devices	WR	1.13 ms	64 devices	
		Batch write	Bit units	BW	1.13 ms	160 devices	2 scans (1 scan when "enable during RUN" is set [excluding R])
			Word devices	WW	1.13 ms	64 devices	
		Test (random write)	Bit units	BT	1.13 ms	20 devices	2 scans (1 scan when "enable during RUN" is set [excluding R])
			Word devices	WT	1.13 ms	10 devices	
		Monitor data registration	Bit units	BM	—	—	—
			Word devices	WM			1 scan for device "R" only
		Monitor	Bit units	MB	2.02 ms	40 devices	1 scan
			Word devices	MN	2.08 ms	20 devices	
	Extension file register	Batch read		ER	1.27 ms	64 devices	2 scan (3 scans for ET [only AnACPU])
		Batch write		EW	1.27 ms	64 devices	
		Test (Random write)		ET	1.31 ms	10 devices	
		Monitor data registration		EM	—	—	—
		Monitor		ME	1.75 ms	20 devices	1 scan
	Buffer memory	Batch read		CR	—	—	—
		Batch write		CW			
Special function module buffer memory		Batch read		TR	FROM instruction processing time + 1.13 msec	128 bytes	1 scan
		Batch write		TW			2 scans (1 scan when "enable during RUN" is set)

Item				Command	Intervening Times (Scan Time Increases)		Scan Count Required for Processing
					A1S	Access Data Unit	
Program	Sequence program	Batch read	Main	MR	1.20 ms	64 steps	1 scan
			Sub	SR	1.20 ms		
		Batch write	Main	MW	0.67 ms		2 scans (1 scan when "enable during RUN" is set)
			Sub	SW	0.67 ms		
	Microcomputer program	Batch read	Main	UR	1.35 ms	128 bytes	2 scans
			Sub	VR	1.35 ms		
		Batch write	Main	UW	1.35 ms		
			Sub	VW	1.53 ms		
	Comment	Batch read		KR	1.35 ms	128 bytes	2 scans
		Batch write		KW	1.53 ms		
	Parameter	Batch read		PR	0.68 ms	128 bytes	2 scans
		Batch write		PW	—	—	—
		Analysis request		PS			
PC CPU		Remote RUN		RR	—	—	—
		Remote STOP		RS			
		PC type read		PC		—	—
Global				GW	—	—	—

POINT

The PC CPU can only process one of these operations with each END processing. If the A6GPP and A1SJ71C24 access a given PC CPU at the same time, one processing must wait until the other processing is completed. Therefore, the scan count required for processing further increases.

APPENDIX 6 SPECIAL FUNCTION MODULE BUFFER MEMORY ADDRESSES

The special function module buffer memory addresses are listed below. They are used to read and write (commands TR, TW) data to and from the special function module buffer memory with protocols 1 to 4.

However, as for the AD70(D), AD71(S1), AD71-S2, or AD72 positioning modules, the buffer area addresses are shown in another section.

The appropriate manuals give details about buffer memory contents.

(1) Linkable special function modules, buffer memory head addresses, and module numbers

Special Function Module Name	Buffer Head Address (Hexadecimal)	Module Number When Loaded in Slot No.0
AD61(S1) high-speed counter module	80H	01H
A616AD analog-digital converter module	10H	01H
A616DAI digital-analog converter module	10H	01H
A616DAV digital-analog converter module	10H	01H
A616TD temperature-digital converter module	10H	01H
A62DA(S1) digital-analog converter module	10H	01H
A68AD(S2) analog-digital converter module	80H	01H
A68ADN analog-digital converter module	80H	01H
A68DAV/DAI digital-analog converter module	10H	01H
A68RD3/4 temperature-digital converter module	10H	01H
A84AD analog-digital converter module	10H	02H
A81CPU PID control module	200H	03H
A61LS position detection module	80H	01H
A62LS position detection module	80H	02H
AJ71PT32 MELSECNET/MINI master module	20H	01H
AJ71C22 multidrop link module	1000H	01H
AJ71C24(S3/S6) computer link module	1000H	01H
AD51(S3) intelligent communications module	800H	02H
AJ71C21(S1) terminal interface module	400H	01H
AJ71B62 B/NET interface module	20H	01H
AJ71P41 SUMINET interface module	400H	01H
AJ71E71 Ethernet interface module	400H	01H

(2) Conversion formula

The addresses specified in the computer (hexadecimal) are converted from FROM/TO instruction addresses as shown below:

Designated address (hexadecimal) = Module head address + [(FROM/TO instruction address x 2) converted into hexadecimal]

The User's Manual of the particular module gives details about the FROM/TO instruction addresses.

6.1 Positioning Module Buffer Memory Addresses

(1) AD71(S1) and AD71-S2 positioning modules

Buffer Memory Contents		Address Set by Computer	Address Set with FROM/TO Instruction
X-axis positioning start data		200H to 391H	0 to 200
Error reset		392H 393H	201
Y-axis positioning start data		458H to 5E9H	300 to 500
Positioning information	X-axis positioning data	2040H to 235FH	3872 to 4271
Positioning velocity	X-axis positioning data	2360H to 267FH	4272 to 4671
Dwell time	X-axis positioning data	2680H to 299FH	4672 to 5071
Positioning address	X-axis positioning data	29A0H to 2FDFH	5072 to 5871
Positioning information	Y-axis positioning data	2FE0H to 32FFH	5872 to 6271
Positioning velocity	Y-axis positioning data	3300H to 361FH	6272 to 6671
Dwell time	Y-axis positioning data	3620H to 393FH	6672 to 7071
Positioning address	Y-axis positioning data	3640H to 3F7FH	7072 to 7871
X-axis parameter		3F80H to 3F9FH	7872 to 7887
Y-axis parameter		3FA8H to 3FC7H	7892 to 7907
X-axis zero return data		3FD0H to 3FDDH	7912 to 7917
Y-axis zero return data		3FE4H to 3FF1H	7922 to 7928

(2) AD72 positioning module

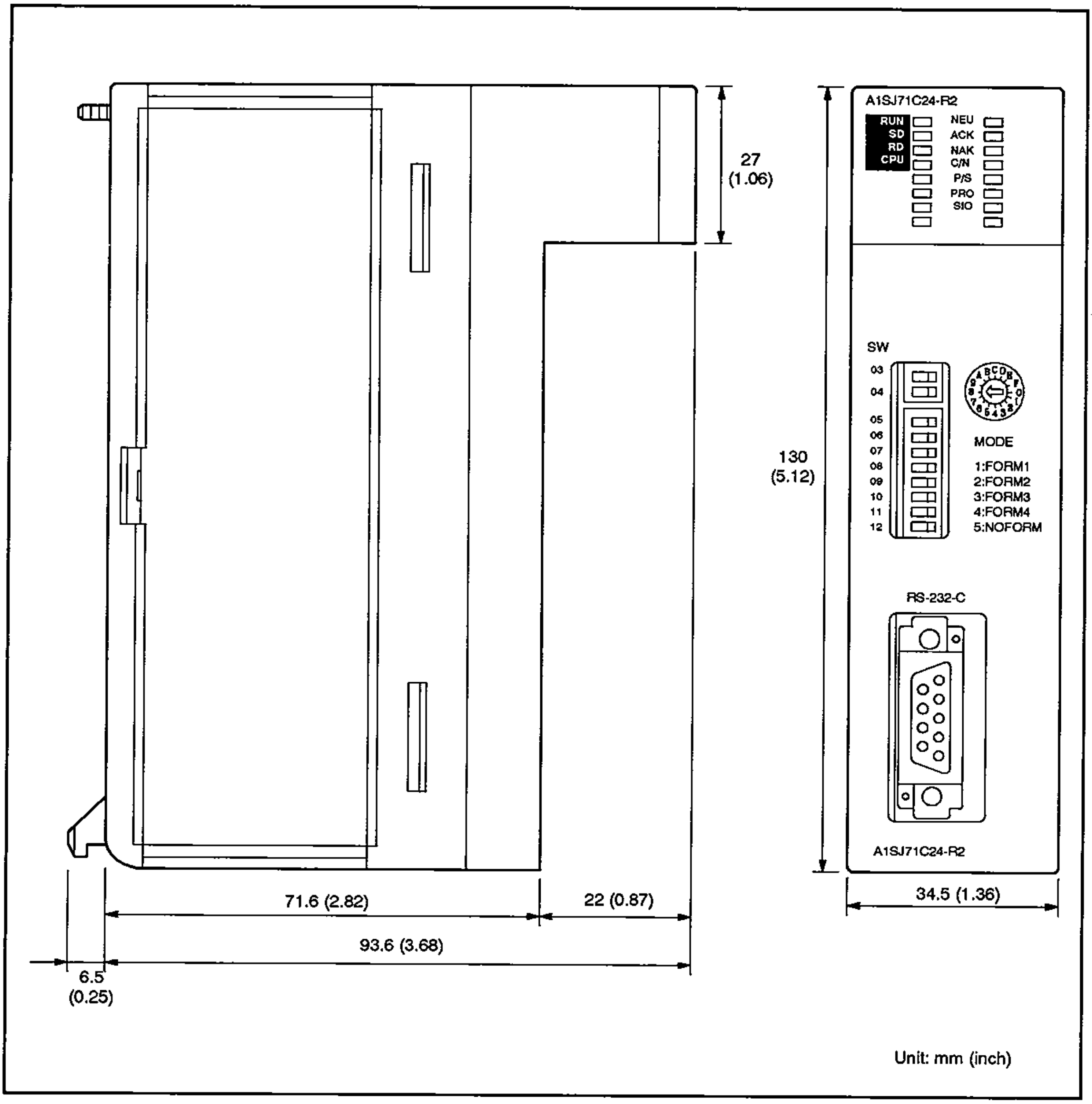
Buffer Memory Contents	Address Set by Computer	Address Set with FROM/TO Instruction
X-axis positioning start data	200H to 391H	0 to 200
Error reset	392H 393H	201
Y-axis positioning start data	458H to 5E9H	300 to 500
Monitor area	6B0H to 6BFH	600 to 607
X-axis positioning data	2040H to 2FDFH	3872 to 5871
Y-axis positioning data	2FE0H to 3F7FH	5872 to 7871
X-axis parameter	3F80H to 3F9FH	7872 to 7891
Y-axis parameter	3FA8H to 3FC7H	7892 to 7911
X-axis zero return data	3FD0H to 3FDDH	7912 to 7917
Y-axis zero return data	3FE4H to 3FF1H	7922 to 7928

(3) AD70 positioning module

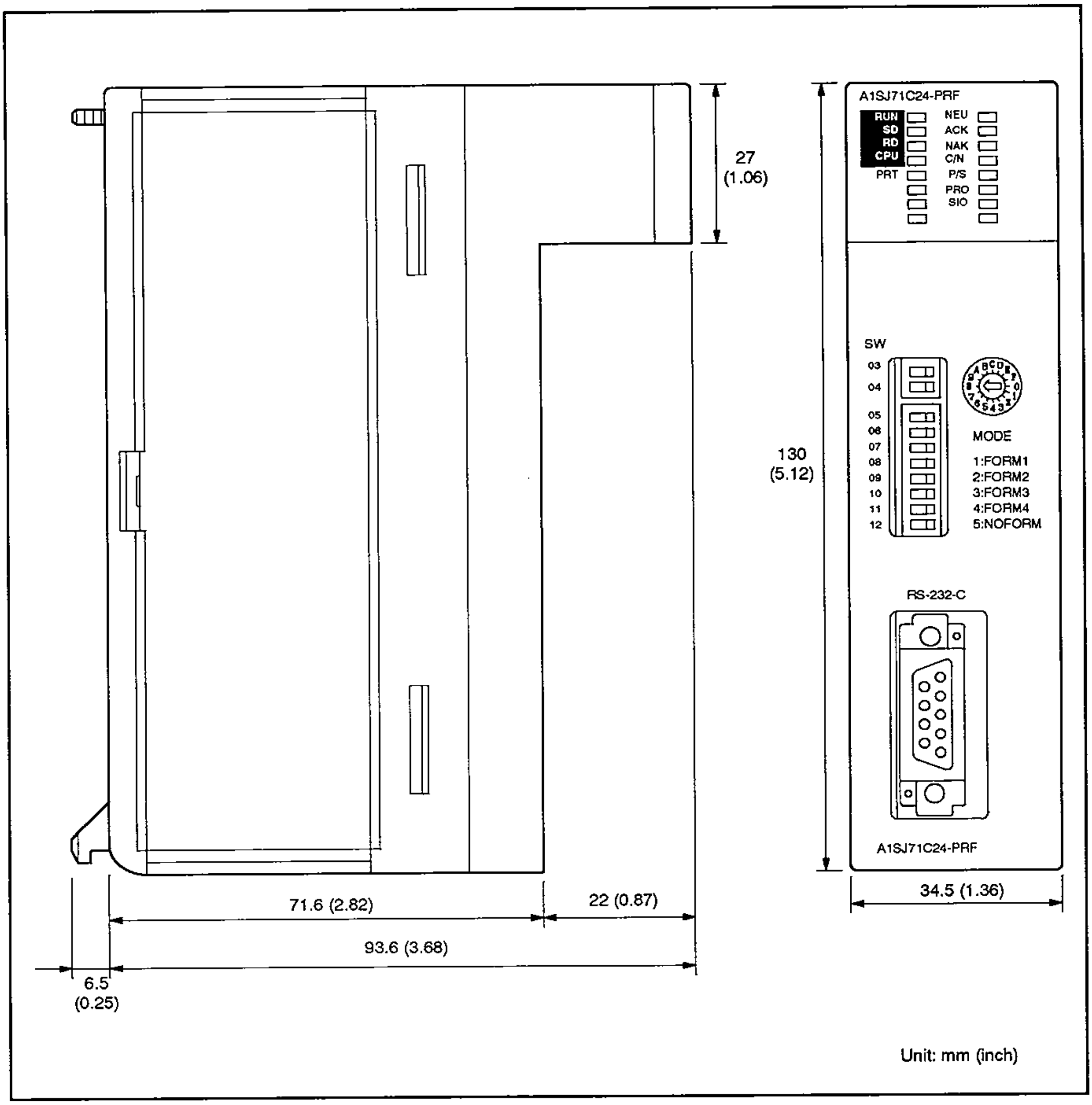
Buffer Memory Contents			Address Set by Computer	Address Set with FROM/TO Instruction
Fixed parameter	Upper stroke limit		80H to 8BH	0 to 5
	Lower stroke limit			
	Electronic gear	Command pulse magnification numerator		
		Command pulse magnification denominator		
Variable parameter	Velocity limit value		A8H to B3H	20 to 25
	Acceleration time			
	Deceleration time			
	In-position range			
	Positioning mode			
Zero return data	Zero point address		D0H to DFH	40 to 47
	Zero return velocity			
	Creep velocity			
	Travel distance setting after near-zero point dog ON			
Positioning data	Positioning pattern		F8H to 109H	60 to 68
	Positioning address P1			
	Positioning velocity V1			
	Positioning address P2			
	Positioning velocity V2			
Control change area	Present value change area		120H to 133H	80 to 89
	Velocity change area			
	JOG velocity area			
	Error counter clear command			
	Analog output adjustment area			
	Velocity position, and travel distance change area			
Monitor area	Feed position data		148H to 15FH	100 to 111
	Actual position data			
	Error code (ERR.1)			
	Error code (ERR.2)			
	Error counter value			
	Travel distance after near-zero point dog ON			
	Velocity position change command			
	n velocity operation			

APPENDIX 7 EXTERNAL VIEW

(1) A1SJ71C24-R2



(2) A1SJ71C24-PRF



APPENDIX 8 A1SJ71C24 SETTING RECORD FORM

Use this form to keep record of settings of the A1SJ71C24 or to create computer link programs for PC CPUs and computers.

Make duplications of this form and use them.

Method of entry

(1) No. and Data

Enter the number of the record form and the date on the top right corner of the form.

(2) Settings of the buffer memory special applications area

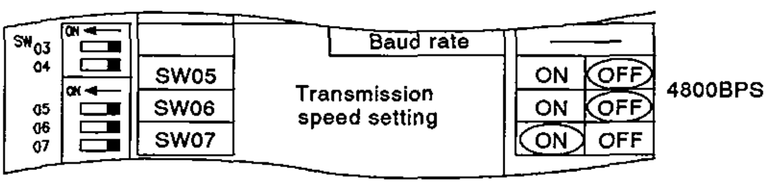
Enter the set values which change default settings when the A1SJ71C24 READY signal (Xn7) is turned ON in the set value's column.

The settings required for the dedicated protocol and the no-protocol/bidirectional mode at the start of the A1SJ71C24 are indicated with [ ] mark in the columns next to the address's column.

(3) Switch settings

(a) Transmission specification switch settings

Circle ON or OFF according to switch setting from SW11 to SW24 in the ON/OFF column.



(b) Mode switch settings

Enter the set value (value indicated by the arrow) in the mode setting switch column.

Record form No. ______ Date ___ : ___ : ___

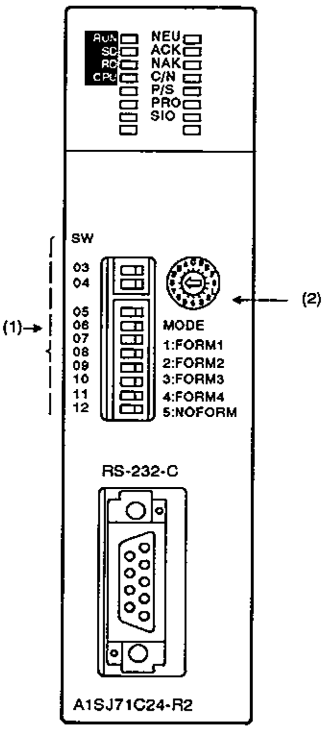
Record of A1SJ71C24 settings

Settings of the buffer memory special applications area	Sections 3.5 and 7 of this manual give details.

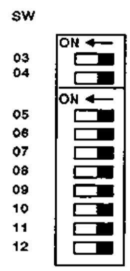
	Address	Dedi-cated Protocol	No-protocol	Bidirec-tional	Printer	Name	Set Value	Default Setting
Buffer memory	100H	—	o	—	—	No-protocol receive-completed code setting area		0D0AH (CR, LF)
	101H	Δ	Δ	Δ	Δ	Error LED ON status storage area	—	0
	102H	o	o	o	o	Error LED turn OFF request area	—	0
	103H	o	o	o	—	No-protocol word byte setting area		0 (words)
	104H	—	o	o	—	No-protocol send buffer memory head address setting area		0
	105H	—	o	o	—	No-protocol send buffer memory length setting area		80H
	106H	—	o	o	—	No-protocol receive buffer memory head address setting area		80H
	107H	—	o	o	—	No-protocol receive buffer memory length setting area		80H
	108H	—	o	—	—	No-protocol receive-completion data length setting area		127 (words)
	109H	—	—	—	—	On-demand buffer memory head address setting area	—	0
	10AH	—	—	—	—	On-demand data length setting area	—	0
	10BH	o	o	o	—	RS-232C CD terminal check setting area	1	0 (check CD enabled)
	10CH	Δ	—	—	—	On-demand error storage area	—	0
	10DH	—	o	—	—	No-protocol received data clear request area	—	0
	10EH	—	—	—	—	System area (unavailable)	—	—
	10FH	o	o	o	—	RS-232C communications mode setting area		0 (Full-duplex)
	110H	o	o	o	—	Simultaneous transmission priority/non-priority setting area		0 (Priority)
	111H	o	o	o	—	Transmission method at transmission resume		0 (Not retransmitted)
	112H	—	—	o	—	Bidirectional mode setting area	1	0 (No-protocol mode)
	113H	—	—	o	—	Time-out check time setting area	100	0 (Infinite)
	114H	—	—	o	—	Simultaneous transmission data valid/invalid setting area		0 (Data valid)
	115H	—	—	o	—	Check sum enable/disable setting area	1	0 (Check sum enabled)
	116H	—	—	Δ	—	Data send error storage area	—	—
	117H	—	—	Δ	—	Data receive error storage area	—	—
	118H	Δ	Δ	Δ	—	Mode setting status storage area		0 (Mode)
	119H	o	o	o	—	Mode switching specification area		0 (No change)
	11AH	—	o	o	o	Transmission control specification area		0 (DTR control)
	11BH	—	o	o	o	DC1/DC3 control code specification area		1311H
	11CH	—	o	o	o	DC2/DC4 control code specification area		1412H

Set value of switch

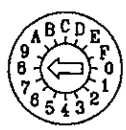
A1SJ71C24-R2



1) Transmission specification setting switch (see Section 4.3.2.).

Switch Setting	Setting Switch	Setting Item		Set Value
	SW03	Unused		ON OFF
	SW04	Write-enabled/disabled setting at RUN		ON OFF
		Transmission speed setting	Baud rate	—
	SW05			ON OFF
	SW06			ON OFF
	SW07			ON OFF
	SW08	Data bit setting		ON OFF
	SW09	Parity bit setting		ON OFF
	SW10	Even/odd parity setting		ON OFF
	SW11	Stop bit setting		ON OFF
	SW12	Sum check		ON OFF

2) Mode setting switch (see Section 4.3.1.).

Mode Setting Switch	Mode Setting Switch No.	Setting	Set Value
 MODE	0	Unusable	
	1	Protocol 1	
	2	Protocol 2	
	3	Protocol 3	
	4	Protocol 4	
	5	No-protocol or printer function	
	6 to E	Unusable	
	F	Used for testing the independent module	

IMPORTANT

(1) Design the configuration of a system to provide an external protective or safety inter locking circuit for the PCs.

(2) The components on the printed circuit boards will be damaged by static electricity, so avoid handling them directly. If it is necessary to handle them take the following precautions.

(a) Ground human body and work bench.

(b) Do not touch the conductive areas of the printed circuit board and its electrical parts with and non-grounded tools etc.

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